

**EIA RS-397-1**

# **EIA STANDARD**

RECOMMENDED STANDARDS  
FOR THYRISTORS

## **RS-397-1**

(Addendum No. 1 to RS-397)



JULY 1980



*Engineering Department*

**ELECTRONIC INDUSTRIES ASSOCIATION**

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RECOMMENDED STANDARDS  
FOR THYRISTORS

(From EIA Standards Proposal No. 1389, formulated under the cognizance of JEDEC JC-22 Committee on Rectifier Diodes and Thyristors.)

This "First Addendum to EIA Recommended Standard RS-397" includes new and/or revised test methods which have been approved by Letter Ballots since 1972.

As a means of merging the supplementary information into the original Standard RS-397, the original indexes to Chapters 5, 6 and 7 have been reproduced wherein the new and/or revised test methods are indicated by means of an asterisk.

## PART 5

### RATINGS ESTABLISHMENT AND VERIFICATION TESTS

#### INDEX

This Addendum forms part of EIA Recommended Standard RS-397. This page is provided to replace page 82 of RS-397. Items asterisked indicate new or revised test methods found in Addendum No. 1.

#### 5.1 Introduction and Reference Table of Ratings and Test Methods

#### 5.2 Electrical Tests

##### 5.2.1 Repetitive Rating Tests

- 5.2.1.1 Steady-State Operational Life Test for Unidirectional Thyristors
- 5.2.1.2 Steady-State Operational Life Test for Bidirectional Thyristors
- 5.2.1.3 Alternating Principal Voltage Life Test
- 5.2.1.4 DC Off-State or Reverse Blocking Voltage Life Test
- 5.2.1.5 Pulsed On-State Current Life Test
- 5.2.1.6 Gate Rating Life Test for Unidirectional Triode Thyristors
- 5.2.1.7 Gate Rating Life Test for Bidirectional Triode Thyristors
- 5.2.1.8 Repetitive Pulse Current Rating Under Specified Turn-Off Conditions Life Test for Reverse Blocking Thyristors
- 5.2.1.9 Thermal Fatigue Life Test for Thyristors

##### 5.2.2 Non-Repetitive Rating Tests

- 5.2.2.1 60 Hz Sine-Wave Surge Current Test and Non-Repetitive Peak Reverse Voltage Test
- 5.2.2.2 Surge (Non-Repetitive) On-State Current, 1.5 Millisecond Duration, Test
- 5.2.2.3 Surge (Non-Repetitive) On-State Current, 0.5 Millisecond Duration, Test
- 5.2.2.4 Rectangular Pulse Surge Current Test
- 5.2.2.5 Peak Positive Anode Voltage Test
- \*5.2.2.6 Critical Rate of Rise of On-State Current Test
- \*5.2.2.7 Destructive Current (Rupture) Test
- \*5.2.2.8 Suppressible Surge Current Test

#### 5.3 Environmental Tests

##### 5.3.1 Storage Life Test

##### 5.3.2 Lead or Terminal Temperature Test

#### 5.4 Post Test Measurements

PART 6  
CHARACTERISTIC TESTS  
INDEX

This Addendum forms part of EIA Recommended Standard RS-397. This page is provided to replace pages 113 and 114 of RS-397. Items asterisked indicate new or revised test methods found in Addendum No. 1.

- 6.1 General
- 6.2 Electrical Measurements - General
  - 6.2.1 Choice of Meters
    - 6.2.1.1 Input
    - 6.2.1.2 Output
  - 6.2.2 Ripple Voltage
  - 6.2.3 Thermal Equilibrium Conditions
    - 6.2.3.1 Steady-State DC Measurements
    - 6.2.3.2 Pulse Measurements
  - 6.2.4 Gate Trigger and Bias Conditions
    - 6.2.4.1 Gate Trigger Pulse
    - 6.2.4.2 Gate Bias
- 6.3 Types of Tests
  - 6.3.1 DC Tests (Static)
    - 6.3.1.1 Test Circuits and Procedures
      - 6.3.1.1.1 DC Breakover Voltage
      - 6.3.1.1.2 DC Reverse Breakdown Voltage
      - 6.3.1.1.3 DC Reverse Blocking Current
      - 6.3.1.1.4 DC Off-State Current
      - 6.3.1.1.5 On-State Voltage
      - 6.3.1.1.6 Latching Current
      - 6.3.1.1.7 DC Holding Current
      - 6.3.1.1.8 Gate Trigger Current and Voltage
      - 6.3.1.1.9 Gate Non-Trigger Current and Voltage
      - 6.3.1.1.10 DC Negative Gate Current
  - 6.3.2 AC Tests (Dynamic)
    - 6.3.2.1 Test Circuits and Procedures
      - 6.3.2.1.1 AC Reverse Blocking Current
      - 6.3.2.1.2 AC Off-State Current
      - 6.3.2.1.3 AC On-State Voltage

PART 6  
CHARACTERISTIC TESTS (continued)

INDEX

- 6.3.3 Instantaneous or Pulse Tests
  - 6.3.3.1 Test Methods
- 6.3.4 Switching Time Tests
  - 6.3.4.1 Gate-Controlled Turn-On Time Test Method
  - 6.3.4.2 Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Thyristors
  - 6.3.4.3 Gate Turn-Off Time Test Method for Gate Turn-Off Thyristors
  - 6.3.4.4 Pulse-Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Triode Thyristors
- 6.3.5 Critical Rate of Rise of Off-State Voltage Test
  - 6.3.5.1 Exponential Voltage Rise Test Method
  - 6.3.5.2 Linear Voltage Rise Test Method
- \*6.3.6 Thermal Resistance and Transient Thermal Impedance Test Method
- \*6.3.7 Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors
- \*6.3.8 Reverse Recovery Characteristics for Thyristors Test Method
- \*6.3.9 Suppressible Surge Current Characteristic

PART 7  
USER'S GUIDE  
INDEX

This addendum forms part of EIA Recommended Standard RS-397. This page is provided to replace page 159 of RS-397. Items asterisked indicate new or revised test methods found in Addendum No. 1.

- 7.1 Introduction
- 7.2 Thyristor Safety Considerations
- 7.3 Voltage Considerations
  - 7.3.1 Basis for Comparison of Thyristor Voltage Ratings
    - 7.3.1.1 Repetitive Peak Reverse Voltage
    - 7.3.1.2 Non-Repetitive Peak Reverse Voltage
    - 7.3.1.3 Repetitive Off-State Voltage
    - 7.3.1.4 Peak Principal Voltage
  - 7.3.2 Overvoltage
  - 7.3.3 Series Operation
- 7.4 Current Considerations
  - 7.4.1 Maximum Operating Junction Temperature
  - 7.4.2 Junction Heat Generation
  - 7.4.3 Thermal Resistance
  - 7.4.4 Steady-State Current Ratings
  - 7.4.5 Overload Current Ratings
  - 7.4.6 Parallel Operation
- 7.5 Triggering
  - 7.5.1 Gate Triggering of Triode Thyristors
  - 7.5.2 Triggering of Diode Thyristors
- 7.6 Switching
  - 7.6.1 Turn-On of Triode Thyristors
  - 7.6.2 Rate-Of-Rise of On-State Current in Triode Thyristors
  - 7.6.3 Turn-On Dissipation
  - 7.6.4 Reverse Recovery
  - 7.6.5 Turn-Off
  - \*7.6.6 Commutation Ability (Bidirectional Thyristors)
- 7.7 Fundamental Thyristor Circuits
- \*7.8 Heat Dissipator Considerations
  - \*7.8.1 General
  - \*7.8.2 Handling Considerations
  - \*7.8.3 Contact Surfaces
  - \*7.8.4 Mounting Torque (Stud Type)
  - \*7.8.5 Clamping Pressure (Disc Type)

PART 7

USER'S GUIDE (continued)

INDEX

This Addendum forms part of EIA Recommended Standard RS-397. Items asterisked indicate new or revised test methods.

- 7.9 Temperature Measurements
  - 7.9.1 General
  - 7.9.2 Ambient Temperature
  - 7.9.3 Thyristor Temperatures
  - 7.9.4 Temperature Measurements Involving Thyristor Mounted on Heat Dissipators
- 7.10 Thyristor Failure Modes
  - 7.10.1 General
  - 7.10.2 Catastrophic Failure
  - 7.10.3 Degradation Failures
- 7.11 Radio Frequency Interference
- 7.12 Simple Measurements in Trouble Shooting
  - 7.12.1 Off-State and Reverse Blocking Voltage Checks
  - 7.12.1 Gate Trigger Check



RECOMMENDED STANDARDS  
FOR THYRISTORS

TABLE OF CONTENTS

<u>Paragraph</u>	<u>Page</u>
5.2.2.6 Critical Rate of Rise of On-State Current Test	1
5.2.2.6.1 Introduction	1
5.2.2.6.2 Test Circuit	1
5.2.2.6.3 Operating Conditions	1-2
5.2.2.6.4 Test Duration	3
5.2.2.6.5 Post Test Measurements	3
5.2.2.7 Destructive Current (Rupture) Rating Test Method	4
5.2.2.7.1 Introduction	4
5.2.2.7.2 Test Method	4
5.2.2.7.3 Operating Conditions	4
5.2.2.7.4 Post Test Measurements	5
5.2.2.8 Suppressible Surge Current Test	7
5.2.2.8.1 Introduction	7
5.2.2.8.2 Test Method	8
5.2.2.8.3 Operating Conditions	8-9
5.2.2.8.4 Post Test Measurements	9

TABLE OF CONTENTS (continued)

<u>Paragraph</u>		<u>Page</u>
6.3.6	Thermal Resistance and Transient Thermal Impedance Test Method	13
6.3.6.1.1	General	13
6.3.6.1.2	Definitions	14
6.3.6.1.3	General Test Description	14
6.3.6.1.4	Heat Dissipator Requirements	16-18
6.3.6.1.5	Determining Reference Temperatures	18-19
6.3.6.2.1	Thermal Resistance Test Method	19
6.3.6.2.1.1	Test Procedure	20-23
6.3.6.2.1.2	Test Circuit	24-26
6.3.6.2.1.3	Test Conditions to be Specified	26
6.3.6.2.1.4	Characteristic to be Determined	27
6.3.6.3.1	Transient Thermal Impedance Test Methods	27
6.3.6.3.1.1	Heating Pulse Method Test Procedure	27-31
6.3.6.3.1.2	Cooling Curve Method Test Procedure	31-35
6.3.6.3.1.3	Test Circuits	35-36
6.3.6.3.1.4	Test Conditions to be Specified	37
6.3.6.3.1.5	Characteristic to be Determined	38
6.3.7	Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors	39
6.3.7.1	Test Description	39
6.3.7.2	Test Circuit	39-40
6.3.7.3	Test Conditions to be Specified	42
6.3.7.4	Characteristic to be Measured	42
6.3.8	Reverse Recovery Characteristics for Thyristors Test Method	43
6.3.8.1	Test Description	43
6.3.8.2	Test Circuit	43-45
6.3.8.3	Waveform of Recovery Current and Definition of Recovery Time	45-46
6.3.8.4	Recovered Charge	46-47
6.3.8.5	Test Conditions to be Specified	47
6.3.8.6	Characteristics to be Measured	48
6.3.9	Suppressible Surge Current Characteristic	52
6.3.9.1	Test Description	52-53
6.3.9.2	Test Circuit	53
6.3.9.3	Test Conditions to be Specified	54
6.3.9.4	Characteristic to be Measured	54

TABLE OF CONTENTS (continued)

<u>Paragraph</u>	<u>Page</u>
7.6      Switching	60
7.6.6    Commutation Ability (Bidirectional Thyristors)	63
7.8      Heat Dissipator Considerations	64
7.8.1    General	64
7.8.2    Handling Considerations	64
7.8.3    Contact Surfaces	64
7.8.4    Mounting Torque (Stud Types)	66
7.8.5    Clamping Pressure (Disc Type)	66-67

## LIST OF FIGURES

<u>Figure</u>		<u>Page</u>
FIGURE 5.2.2.6-1	Basic Test Circuit for the Critical Rate of Rise of On-State Current Test	2
FIGURE 5.2.2.6-2	On-State Current Waveshape for the Critical Rate of On-State Current Test	3
FIGURE 5.2.2.7-1	Fault Test Circuit	6
FIGURE 5.2.2.8-1	Basic Test Circuit for Suppressible Surge Current Rating Test	10
FIGURE 5.2.2.8-2	Current and Voltage Waveform applied to the Device Under Test	10
FIGURE 6.3.6-1	Typical Transient Thermal Impedance Characteristic	16
FIGURE 6.3.6-2	Current and Voltage Waveforms During Thermal Resistance Test	21
FIGURE 6.3.6-3	Illustration of On-State Voltage Waveform Extrapolation	22
FIGURE 6.3.6-4	Thermal Resistance Test Circuit	25
FIGURE 6.3.6-5	Current and Voltage Waveform for Transient Thermal Impedance Test	30
FIGURE 6.3.6-6	Reference Temperature $T_{R1}$	34
FIGURE 6.3.6-7	Basic Test Circuit for Transient Thermal Impedance Test Method	35
FIGURE 6.3.7-1	Test Waveforms	41
FIGURE 6.3.7-2	Critical Rate of Rate of Rise Commutation Voltage Test Circuit	42
FIGURE 6.3.8-1	Circuit for Measuring Reverse Recovery Characteristics for Thyristors	49
FIGURE 6.3.8-2	Test Circuit for Measuring Reverse Voltage Recovery Characteristics of Thyristors	50
FIGURE 6.3.8-3	Reverse Recovery Current Waveform for Various Type of Thyristors	51
FIGURE 6.3.9-1	Basic Test Circuit for Suppressible Surge Current Characteristic Test	55
FIGURE 6.3.9-2	Current and Voltage Waveforms Applied to the Device under Test	55

## 5.2.2.6 Critical Rate of Rise of On-State Current Test

### 5.2.2.6.1 Introduction

The rate at which on-state current can be increased in a thyristor is limited by the initial turned on area and the rate of increase and modulation of the active area during turn on. This test method may be used to apply a rate of rise of on-state current ( $di/dt$ ) stress to a triode thyristor for the purpose of establishing a rating. This rating is necessary for those devices unable to withstand the rate of rise of on-state current determined by their turn-on characteristics in a non-inductive circuit.

This rating may be either repetitive or non-repetitive which means respectively that the rating may be applied an unlimited or a limited number of times. Two different non-repetitive ratings may be assigned to triode thyristors: one for gate triggering and one for triggering by exceeding the thyristor breakover voltage. The time between on-state current pulses in the non-repetitive rating case shall be long enough to insure that the device temperature has returned to its original thermal equilibrium. For bidirectional devices, these ratings apply for operation in either quadrant.

### 5.2.2.6.2 Test Circuit

A suitable test circuit is shown in Fig. 5.2.2.6-1. The  $di/dt$  stress is applied using the device under test to discharge a capacitor through a series resistor and inductor to produce a damped on-state current pulse. Reverse switching transients may be suppressed as this method is intended to be a test of on-state switching capability only. Approximate values of  $R$ ,  $L$  and  $C$  in terms of the test conditions are given in Fig. 5.2.2.6-1. For those values of circuit constants to apply in the case of breakover voltage triggering,  $V_{DM}$  is replaced by the  $V_{(BO)}$  of the test device.

### 5.2.2.6.3 Operating Conditions

5.2.2.6.3.1 Fig 5.2.2.6-2 illustrates the on-state current wave shape, and identifies several test conditions.

Zero time is determined by the intersection, with the time axis, of the straight line passing through the 10% and 50% test current.

- 5.2.2.6.3.2 The time  $t_1$  shall be  $\geq 1$  microsecond.
- 5.2.2.6.3.3  $I_{TM}$  shall be  $\geq$  twice the rated value of on-state current at  $T_3$ . (The rated value of on-state current at  $T_3$  will be an average value for ac rated devices and a dc value for dc rated devices).
- 5.2.2.6.3.4 The pulse repetition rate for establishment of the repetitive rating for unidirectional thyristors and for bidirectional thyristors shall be 60 p/s.
- 5.2.2.6.3.5 The off-state voltage  $V_{DM}$ , when applicable, shall be equal to the rated value at  $T_5$ .
- 5.2.2.6.3.6 The temperature shall be  $T_5$ .
- 5.2.2.6.3.7 The gate trigger pulse, when applicable, shall be specified as to:
- Pulse width,  $t_w$
  - Rise time,  $t_r$
  - Gate source voltage and resistance

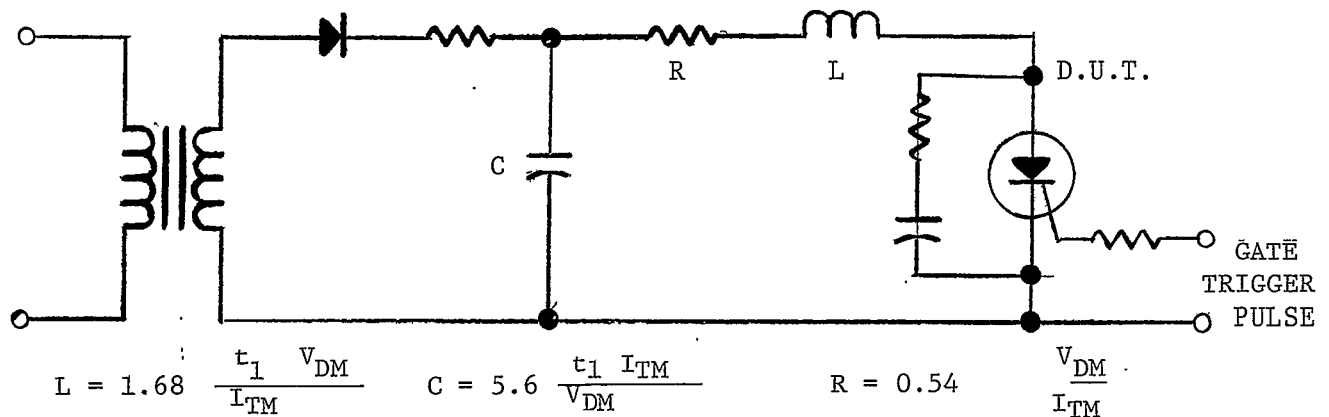


FIGURE 5.2.2.6-1-BASIC TEST CIRCUIT FOR THE CRITICAL RATE OF RISE OF ON-STATE CURRENT TEST

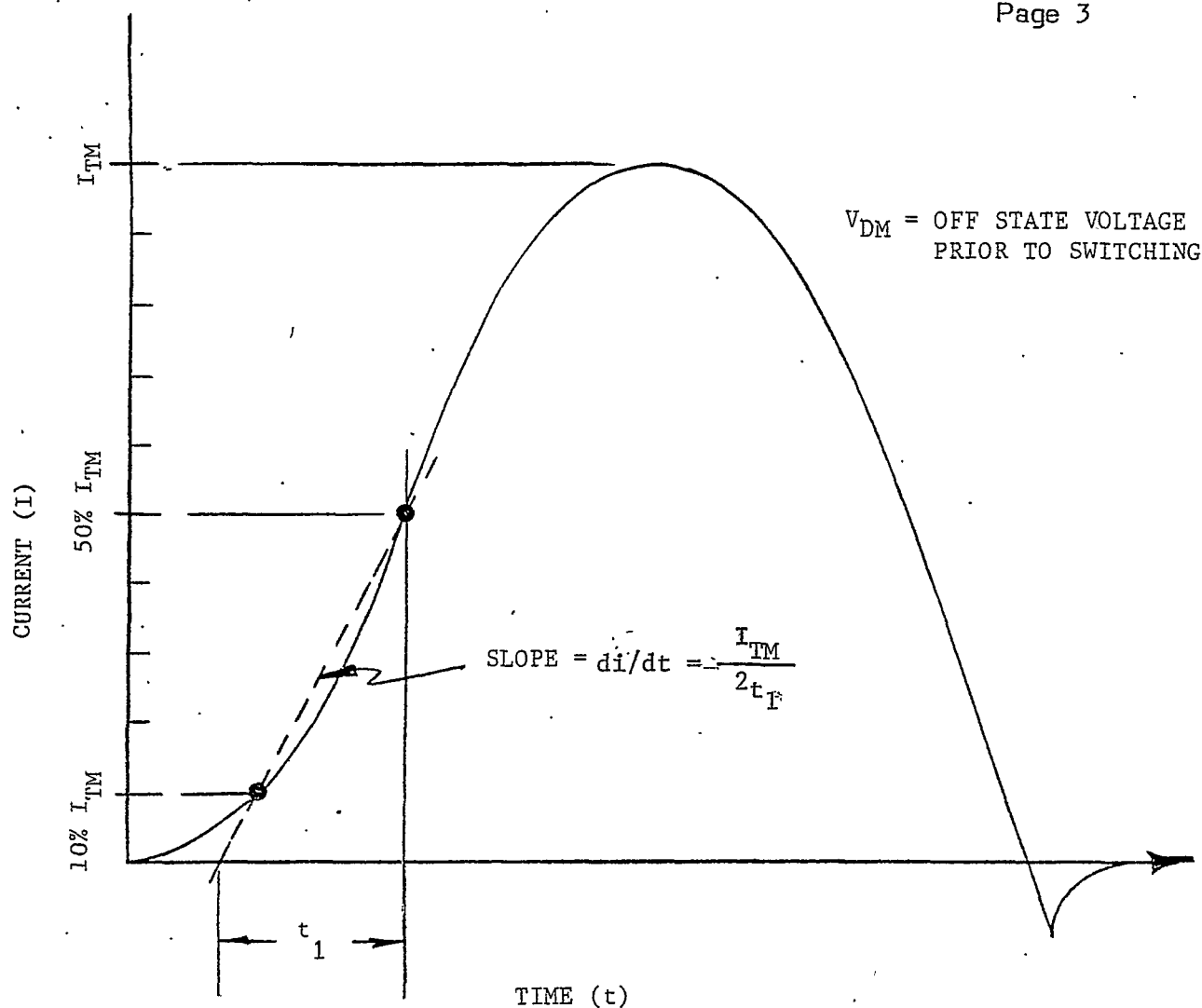


FIGURE 5.2.2.6-2 ON-STATE CURRENT WAVESHAPE FOR THE CRITICAL RATE OF RISE OF ON-STATE CURRENT TEST

#### 5.2.2.6.4 Test Duration

- 5.2.2.6.4.1 The test duration shall be 1000 hours in establishing the repetitive rating.
- 5.2.2.6.4.2 The number of on-state current pulses shall be 100 in establishing the breakover-voltage-triggered non-repetitive rating.
- 5.2.2.6.4.3 The number of on-state current pulses shall be 300 at a 60 Hz repetition rate in establishing the gate-triggered non-repetitive rating.

#### 5.2.2.6.5 Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

## 5.2.2.7 Destructive Current (Rupture) Rating Test Method

### 5.2.2.7.1 Introduction

This test method is used to establish the maximum overload current that a thyristor (except on bidirectional types) can withstand without rupturing the device package. The device is electrically shorted by exceeding the device reverse breakdown voltage with a low energy pulse such that the failure location is on the device periphery near the active area. Other failure modes, such as di/dt, gate power, bulk voltage breakdown, or required open circuit between anode and cathode terminals, are not the subject of this test method.

### 5.2.2.7.2 Test Method

Initially the test device is ascertained to be hermetic (Leak Rate  $\leq 1 \times 10^{-6}$  atm cm<sup>3</sup>/s)\* and to be an electrical short in the blocking junction(s) on the periphery of the device.

The test device is mounted in a fixture per the manufacturer's recommended mounting procedure. At these high current levels, the location and rigidity of mounting is important since tremendous magnetic forces could alone cause assembly damage and loosening of hardware.

### 5.2.2.7.3 Operating Conditions

The circuit shown in Figure 5.2.2.7-1 is one means to generate current levels to cause rupture. A high voltage alternator is used to give a short term power capability in excess of 470,000 kVA. The test device is located in the secondary of the transformer in series with a fuse.

The magnitude and shape of the peak let-thru current is determined by fuse selection. The series fuse is used to limit the selected peak let-thru current. The asymmetry is controlled by a pilot alternator on the same shaft with the main alternator. The output of the pilot device is fed into electronic circuitry which controls the closing device. The back-up breakers perform when the closing device fails to operate from its overcurrent trip.

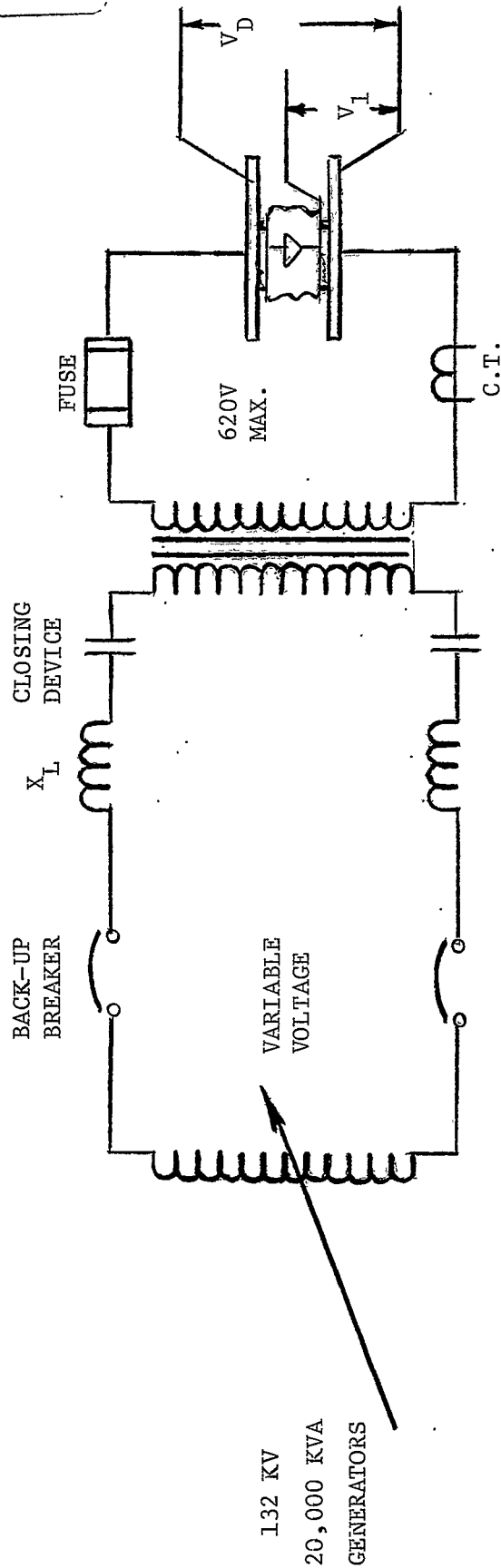
\*Often written " $1 \times 10^{-6}$  atm cc/s".



- 5.2.2.7.3.1 The power shall be from a 60Hz sinusoidal waveform source with fault current applied in the reverse direction to the reverse blocking junction.
- 5.2.2.7.3.2 The initial device case temperature will be 25°C.
- 5.2.2.7.3.3 Gate bias condition shall be open (for thyristors only).
- 5.2.2.7.3.4 No peak reverse voltage is necessary after the destructive half-sine wave of current is interrupted.
- 5.2.2.7.3.5 The number of destructive current surges to be applied shall be 1.
- 5.2.2.7.3.6 The peak destructive current and the fault clearing time causing rupture shall be defined.

5.2.2.7.4 Post Test Measurements

The hermetic leak rate test shall be repeated on a device which has been rupture current tested. A device is defined as ruptured if there is a visible puncture in the package or if the leak rate exceeds  $1 \times 10^{-6}$  atm cm<sup>3</sup>/s.



FAULT TEST CIRCUIT

FIGURE 5.2.2.7-1

## 5.2.2.8 Suppressible Surge Current Test

### 5.2.2.8.1 Introduction

This test is used to varify suppressible surge current ratings for reverse blocking triode thyristors. Unlike the non-repetitive 60 Hz Surge Current Rating ( $I_{TSM}$ ), this test requires the device to maintain off-state voltage blocking capability after the surge current interval. Primarily intended for SCR's in high power systems. This type of rating is needed in applications where the thyristor is subjected to random short circuit loads and then is required to sustain off-state voltage immediately following circuit voltage reversal.

As in most surge or fault situations the junction temperature of the device may exceed (during the surge current interval) the maximum allowable steady junction temperature. In this suppressible surge current rating the critical parameter is the device junction temperature at the time off-state voltage is reapplied. Depending on the junction temperature at this critical time, device characteristics may be a primary factor in determining the suppressible surge current rating. These characteristics are gate trigger current and voltage turn-off time, leakage current, and  $dv/dt$ .

The junction temperature at the critical time the off-state voltage is reapplied will be primarily determined by the case temperature, the magnitude of the steady-state load current and the magnitude, shape and duration of the surge current. The time between the end of the surge current and the application of reapplied off-state voltage will also influence this temperature.

The test device is brought up to a specified steady-state case temperature by means of a heated test fixture. The time between on-state current surges should be long enough to permit the device virtual junction temperature to return to its original thermal equilibrium value. The device under test should be triggered with sufficient gate drive to ensure full turn on.

#### 5.2.2.8.2 Test Method

This test circuit to be used is shown in Figure 5.2.2.8-1 and voltage and current waveforms are shown in Figure 5.2.2.8-2.

The specified repetitive peak 60 Hz sine wave reverse and off-state voltages are applied to the test device. The surge current pulse and reapplied reverse and off-state voltages are controlled by SCR's 1, 2 and 3 in the test circuit. Sufficient delay should be provided in the triggering of SCR 3 to assure that SCR1 is fully off.

The time from the end of the on-state surge current ( $t_1$ ) to the beginning of the off-state voltage waveform ( $t_2$ ) shall be specified. This time ( $t_2 - t_1$ ) can be varied in rough steps by proper selection of two phases of a three phase incoming line. The times that can be so obtained are approximately 2.2, 5.0 and 7.7 ms with 7.7 ms being the value obtained when both input transformers are connected to the same phase, the value of 7.7 ms is recommended. Circuit B (Figure 5.-. may be used to obtain continuous adjustment.)

The reapplied off-state voltage should be observed on an oscilloscope to determine that the device blocks the first half cycle of off-state voltage following the surge current. Failure of the device to block the reapplied off-state voltage following the current surge indicates the device has not passed the test.

#### 5.2.2.8.3 Operating Conditions

1. The power sources shall be a 60 Hz sinusoidal waveform sources.
2. The specified value of suppressible surge current amplitude shall be used.
3. The specified value of suppressible surge current amplitude pulse width ( $t_1 - t_0$ ) shall be between 8.3 and 9.5 ms (asymmetric half sine wave).

5.2.2.8.3 Operating Conditions Cont'd.

4. Time from the end of the on-state surge current pulse ( $t_1$ ) to the beginning of the off-state voltage waveform ( $t_2$ ) shall be as specified ( $t_2 - t_1$ ).
5. The magnitude of the off-state voltage shall be as specified.
6. The case temperature prior to the surge current waveform shall be as specified. This temperature shall be maintained by a heated test fixture.
7. Gate conditions following the surge current shall be as specified.
8. The test device shall be mounted under minimum rated mounting force or torque conditions.
9. The minimum time between surge-current pulses shall be 1 minute, unless thermal equilibrium is achieved in a shorter time.
10. The number of surge current pulses to be applied shall be 1,000.

5.2.2.8.4 Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

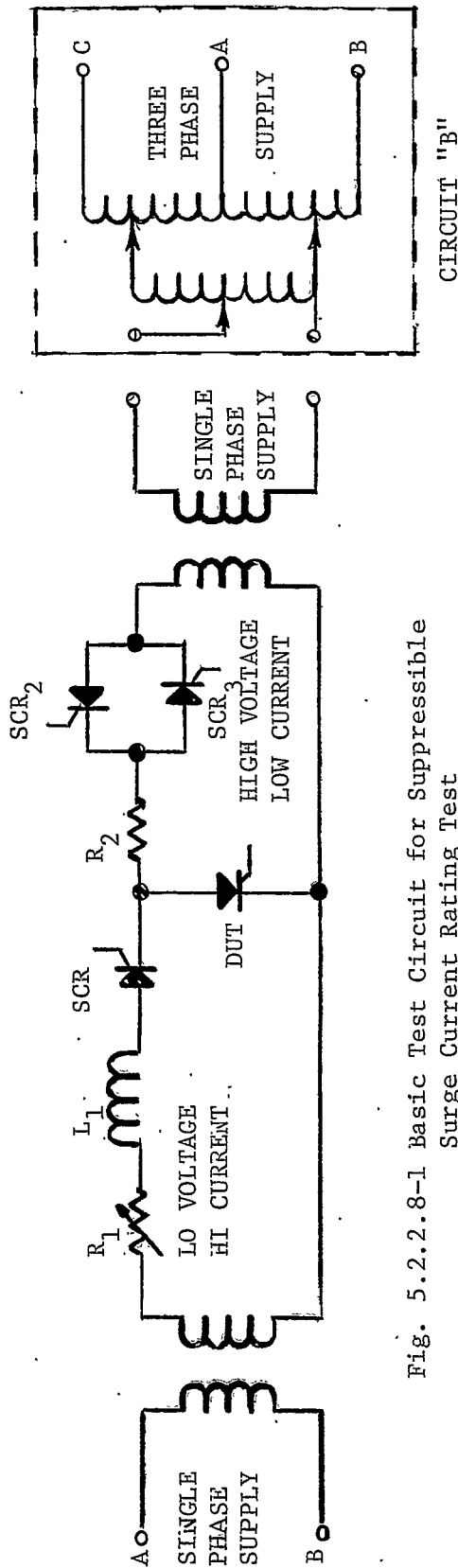
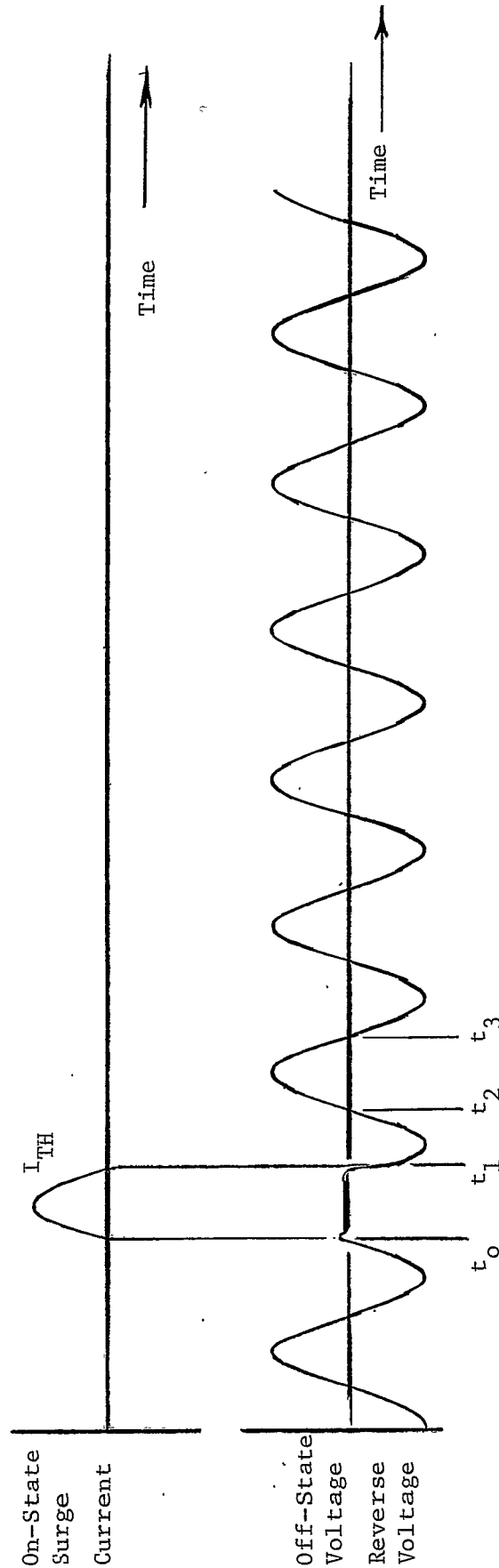


Fig. 5.2.2.8-1 Basic Test Circuit for Suppressible Surge Current Rating Test



- $t_1 - t_0$  Duration of on-state surge current pulse.
  - $t_2 - t_1$  Time between end of surge current pulse and start of reapplied off-state voltage.
  - $t_3 - t_2$  Duration of reapplied off-state voltage.
- Fig. 5.2.2.8-2 Current and Voltage Waveform applied to the Device Under Test

PART 6  
CHARACTERISTIC TESTS  
INDEX

- 6.1 General
- 6.2 Electrical Measurements - General
  - 6.2.1 Choice of Meters
    - 6.2.1.1 Input
    - 6.2.1.2 Output
  - 6.2.2 Ripple Voltage
  - 6.2.3 Thermal Equilibrium Conditions
    - 6.2.3.1 Steady State DC Measurements
    - 6.2.3.2 Pulse Measurements
  - 6.2.4 Gate Trigger and Bias Conditions
    - 6.2.4.1 Gate Trigger Pulse
    - 6.2.4.2 Gate Bias
- 6.3 Types of Tests
  - 6.3.1 DC Tests (Static)
    - 6.3.1.1 Test Circuits and Procedures
      - 6.3.1.1.1 DC Breakover Voltage
      - 6.3.1.1.2 DC Reverse Breakdown Voltage
      - 6.3.1.1.3 DC Reverse Blocking Current
      - 6.3.1.1.4 DC Off-State Current
      - 6.3.1.1.5 On-State Voltage

- 6.3.1.1.6 Latching Current
- 6.3.1.1.7 DC Holding Current
- 6.3.1.1.8 Gate Trigger Current and Voltage
- 6.3.1.1.9 Gate Non-Trigger Current and Voltage
- 6.3.1.1.10 DC Negative Gate Current
- 6.3.2 AC Tests (Dynamic)
  - 6.3.2.1 Test Circuits and Procedures
    - 6.3.2.1.1 AC Reverse Blocking Current
    - 6.3.2.1.2 AC Off-State Current
    - 6.3.2.1.3 AC On-State Voltage
- 6.3.3 Instantaneous or Pulse Tests
  - 6.3.3.1 Test Methods
- 6.3.4 Switching Time Tests
  - 6.3.4.1 Gate-Controlled Turn-On Time Test Method
  - 6.3.4.2 Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Thyristors
  - 6.3.4.3 Gate Turn-Off Time Test Method for Gate Turn-Off Thyristors
  - 6.3.4.4 Pulse-Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Triode Thyristors
- 6.3.5 Critical Rate of Rise of Off-State Voltage Test
  - 6.3.5.1 Exponential Voltage Rise Test Method
  - 6.3.5.2 Linear Voltage Rise Test Method
- \*6.3.6 Thermal Resistance and Transient Thermal Impedance Test Method
- 6.3.7 Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors
  - \*6.3.7.1 Test Description
- \*6.3.8 Reverse Recovery Characteristics for Thyristors Test Method
- \*6.3.9 Suppressible Surge Current Characteristic



### 6.3.6 Thermal Resistance and Transient Thermal Impedance Test Method

#### 6.3.6.1.1 General

This test method applies to reverse conducting and reverse blocking triode thyristors, and to bidirectional triode thyristors when applied independently for each polarity of operation.

The thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure to provide for heat removal from the active semiconductor element. Therefore, thermal resistance is an important factor in establishing the power handling ability of a semiconductor device.

The transient thermal impedance of a semiconductor device is a measure of the ability of its mechanical structure to provide for heat storage as well as heat removal from the active semiconductor element. Therefore, transient thermal impedance is an indication of the short pulse-duration power handling ability of a semiconductor device.

One dimensional heat flow is assumed in thermal resistance and transient thermal impedance specifications and such specifications must always include the two points or planes between which the thermal resistance or transient thermal impedance value applies. The term virtual junction temperature is here applied to multi-junction devices to indicate the temperature of the active semiconductor element for use in the device test methods and specifications. The reference temperature is usually established at one of the following:

1. A specified point on the case.
2. A specified point on a lead.
3. The ambient air.

When the semiconductor may be either single- or double-side cooled, as with a disc or axial lead package, the applicable type of cooling must be specified.

#### 6.3.6.1.2 Definitions

Thermal resistance of a semiconductor device is defined as the temperature difference between two specified points or regions of the device divided by the power being dissipated which causes the temperature difference under conditions of thermal equilibrium.

Transient thermal impedance of a semiconductor device is defined as the change in temperature difference between two specified points or regions of the device at the end of a time interval divided by the step function change in power dissipation which causes the change in temperature divided by the step function change in power dissipation which causes the change in temperature difference during the same time interval.

#### 6.3.6.1.2 General Test Description

Since virtual junction temperature is difficult to measure directly, a temperature sensitive device parameter is used as its indicator. On-state voltage at a small percentage of rated current  $V_{T(MET)}$  is the parameter used. The corresponding value of the low level on-state current used in this test method is called metering current,  $I_{T(MET)}$ .

To measure thermal resistance, ( $R_{\theta JR}$ ) or transient thermal impedance ( $Z_{\theta JR}$ ) measurements are taken to satisfy the appropriate equations:

$$R_{\theta JR} = \frac{T_J - T_R}{P(AVG)} = \frac{T_{R1} - T_{R2}}{V_{T(HTG)} \times I_{T(HTG)} \times \text{Duty Factor}}$$

$$R_{\theta JR} = \frac{T_J - T_R}{\text{Peak Power}} = \frac{T_{R1} - T_{R2}}{V_{T(HTG)} \times I_{T(HTG)}}$$

where:

$T_{R1}$  = measured reference (case, lead or ambient) temperature with only metering current flowing. It is that temperature (obtained by adjusting externally applied heat) which produces a value of low level on-state voltage (called metering voltage) which is equal to that obtained in the test set immediately following device operation with power applied. Note that  $T_{R1}$  is therefore essentially the same as the device virtual junction temperature.

$T_{R2}$  = measured reference (case, lead or ambient)  
temperature when operated with power applied.

$I_{T(HTG)}$  = Heating current used to produce the power  
dissipated in the active element of the diode.

$V_{T(HTG)}$  = Measured value of on-state voltage when  
 $I_{T(HTG)}$  is applied.

Data to calculate thermal resistance is obtained by using a switching circuit which applies pulsed power at a high duty factor. The metering current is maintained for short periods during which the metering voltage is read out, and from this the virtual junction temperature at the end of each power pulse is determined.

Two methods may be used to determine transient thermal impedance, a heating pulse method and a cooling method. A typical transient thermal impedance curve is shown in Figure 6.3.6-1.

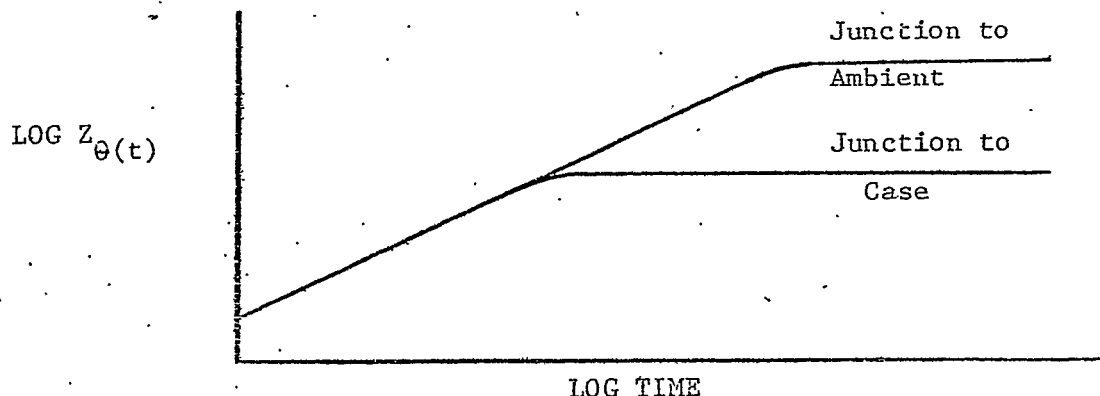


FIGURE 6.3.6-1 - TYPICAL TRANSIENT THERMAL IMPEDANCE CHARACTERISTIC

Although the curve represents the junction temperature response to heating provided by the application of single rectangular power pulses of specified time durations, the curve can be arrived at from the cooling curve of the active semiconductor element following interruption of continuously applied steady-state power. This cooling method is generally recommended for high current thyristors since it is easier to perform than the heating pulse method which requires very high level power pulses to give significant junction temperature rise, particularly for short pulse durations.

Since measurement of thermal resistance, or of transient thermal impedance by the cooling method involves high average power levels, considerable attention must be given to the heat dissipator used and the thyristor mounting arrangement.

#### 6.3.6.1.4 Heat Dissipator Requirements

The recommended type of heat dissipator for the junction-to-case thermal resistance test on stud-mounted thyristors is a flat plate with the test device centrally mounted on it. For stud types, the mounting shall be through a clearance hole in the plate with the device fastened by means of a nut. The clearance hole in the plate should only be large enough to allow free passage of the stud. The plate thickness should be no more than one-half the stud diameter. The mounting surface should be flat, burr-free, etc., as described in Part 7 of this standard. The device should be mounted using the manufacturer's recommendations regarding torque values, thread lubricants (or absence of same) and thermal compound applied to the device and heat dissipator interface.

For base-mounted thyristors, a similar flat plate should be used, drilled to accept the mounting hardware required by the DUT. The plate thickness should be the same as it would be for a stud-mounted thyristor of similar mounting dimensions at the seating plane.

The conductor connected to the top terminal of a stud- or base-mounted thyristor should be such that its heat dissipation does not add to the virtual junction temperature of the thyristor under test. For solder terminal devices, it is recommended that the wire size used be the largest that will fit through the hole in the terminal. A bare conductor of this size doubled back to its point of origin is recommended. Devices with flexible top leads should have the lead bolted to a heavy copper bus. There should be no forced air cooling of the device case, lead or terminal.

The recommended type of heat dissipator for the junction-to-lead thermal resistance test on axial lead type devices is two flat plates with the test device centrally mounted. The plate thickness should be no more than the device lead diameter. The device should be mounted using the manufacturer's recommendations regarding surface preparation and electrical and thermal bonding between device leads and heat dissipators.

If forced air cooling is used, the cooling air should blow over the dissipators only and the device case and lead structures should be isolated. The connections to the leads should be such that heat dissipated there does not add to the virtual junction temperature of the device under test; similarly, the leads should not be cooled so as to remove heat from the device.

If natural convection cooling is used, the following conditions must be met:

- (a) The thyristor shall be mounted horizontally in a cubic enclosure of volume of not less than 1 cubic foot. If the thyristor is mounted on a heat dissipator, e.g., a square metal plate, it should be suspended vertically in the cubic enclosure. Each dimension of the enclosure should be a minimum of four times the dissipator height.

- (b) There shall be no radiation sources in the enclosure other than the device under test.
- (c) The interior enclosure wall shall have a low reflectance finish (emissivity = 1.0\* (approximately))
- (d) The thyristor shall be mounted in such a manner that conduction cooling through the leads or the sockets or both shall be small compared to the other cooling mechanisms.
- (e) More than one thyristor may be put in the enclosure, but all must be mounted on the same horizontal plane, and they shall be at least five case dimensions away from each other and from the walls. Only one thyristor may be energized at a time.

It is recommended that a water cooled heat dissipator be used with disc type thyristors. Thermal compound shall be applied between the thyristor pole pieces and the mounting surfaces of the heat dissipator(s), which shall be flat and smooth. The mounting force recommended by the device manufacturer shall be applied perpendicularly to the thyristor pole pieces using a recommended clamping arrangement.

Since thermal resistance is affected somewhat by junction temperature, it is recommended that the thermal resistance test be performed so that the test device virtual junction temperature is within 20% of its maximum rated value. The size of the heat dissipator used for the power application test must be chosen to accomplish this or a controlled temperature system must be employed. The approximate case, lead or ambient temperature,  $T_{R2}$ , at which the device must be operated can be determined from the basic thermal resistance equation.

The ambient temperature should be measured by means of a thermocouple mounted at a distance approximately 0.5 inch directly beneath the device under test.

#### 6.3.6.1.5 Determining Reference Temperatures

##### Stud- and Base-Mounted Thyristors

The measurement of both  $T_{R1}$  and  $T_{R2}$  is made by means of a thermocouple attached to the device case specified reference point. See Section 7 of EIA Standard RS-397 for details on reference points and methods of thermocouple attachment.

### Lead Mounted Thyristors

The measurement of both  $T_{R1}$  and  $T_{R2}$  is made by means of a thermocouple attached to the thyristor on either the anode (or MT2) or the cathode (or MT1) lead at the specified reference point. See Section 7 of EIA Standard RS-397 for methods of thermocouple attachment.

### Disc Type Thyristors

Single Side Cooling: The disc type device is mounted between a flat plate of minimum size and thickness and a heat dissipator which is usually liquid cooled. See Part 7 of EIA Standard RS-397 for methods of thermocouple attachment. The anode (or MT2) is cooled by placing the anode (or MT2) side of the thyristor against the heat dissipator while the opposite (cathode, or MT1) side is not cooled.  $T_{R1}$  and  $T_{R2}$  are obtained from a thermocouple located in the anode (or MT2) pole piece.

To measure the thermal resistance with the cathode side cooled, the disc type thyristor is removed, turned over and remounted. The thermocouple used to obtain  $T_{R1}$  and  $T_{R2}$  is now located in the cathode (or MT1) pole piece of the thyristor.

Double Side Cooling: The disc type thyristor is placed between two heat dissipators of equal cooling efficiency with thermocouples for measuring  $T_{R1}$  and  $T_{R2}$  on both the anode (or MT2) and cathode (or MT1) pole pieces. Thermal resistance based on both the anode (or MT2) pole piece and the cathode (or MT1) pole piece thermocouple readings should be obtained and then averaged to determine the double side cooled thermal resistance. Alternately, single side cooled values of  $T_{R1}$  and  $T_{R2}$  can be used to calculate the double side cooled value by using a parallel thermal resistance analog.

#### 6.3.6.2.1 Thermal Resistance Test Method

The test procedure consists of two distinct steps: A power application test and a calibration test.

#### 6.3.6.2.1.1 Test Procedure

##### Step 1 - Power Application Test

First, the thyristor is operated with power intermittently applied by a very high duty cycle. During the intervals between power pulses (when the heating current has been removed), the metering current continues to flow and the on-state voltage is measured. The thyristor current and voltage waveforms are shown in Figure 6.3.6-2 for a 60 Hz repetition rate testing very high current devices, a slower repetition rate may be required (thereby lengthening time interval  $t_1 - t_4$ ) in order that the interval  $t_4 - t_1$  can be made greater than .333 millisecond and still meet the requirement of a minimum duty factor of 98 percent. The metering current which flows continuously must be held constant. This is particularly important during the metering interval between power pulses because the test device impedance will vary considerably during that time.

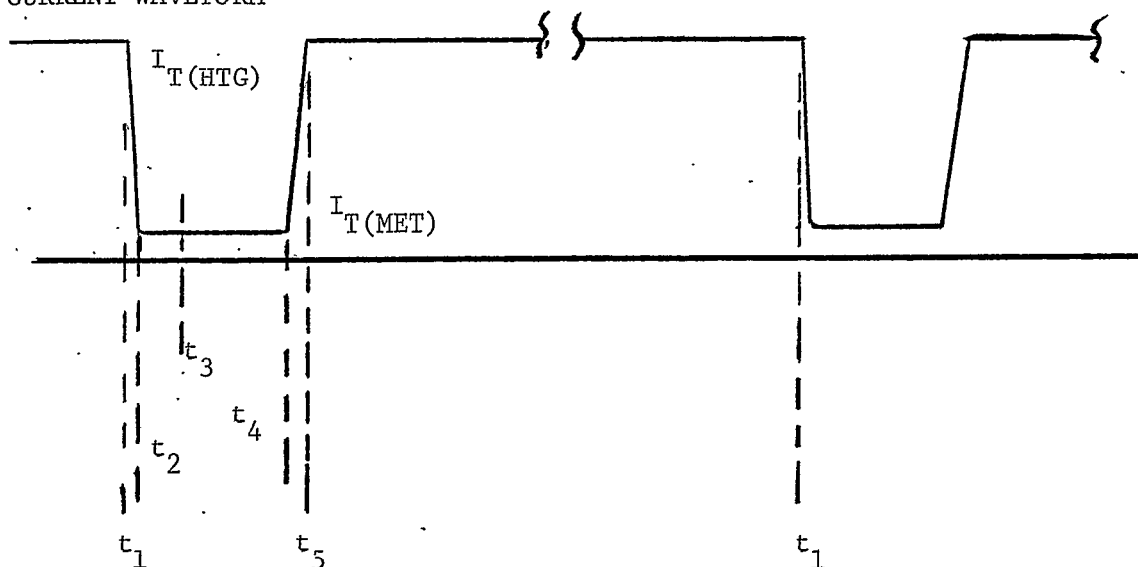
It would be desirable to arrive at the thyristor virtual junction temperature at the exact instant when the heating current removal is initiated since the virtual junction temperature will be maximum at that time. However, this is not possible by direct measurement. First it takes a finite time for the thyristor current to decay from the heating current value to the metering current value ( $t_2 - t_1$  in Figure 6.3.6-2.) This fall time must be controlled and the rate of on-state current decay is listed as a test condition. Secondly, transients will exist in the on-state voltage waveform for some time after the metering current value has been reached. These induced voltages are due primarily to the reduction in on-state current and may also cause some on-state voltage waveform distortion.



6.3.6.2.1.1 (continued)

Consequently the on-state voltage cannot be used as an indicator of virtual junction temperature until after these transients have subsided.

(A) CURRENT WAVEFORM



$$t_4 - t_1 = 0.333 \text{ ms}$$

$$t_1 - t_1 = 16.7 \text{ ms}$$

$$\text{Duty Cycle} = 0.98$$

$$I_{T(MET)} = \text{Metering Current}$$

$$I_{T(MET)} = \text{Heating Current}$$

$$V_T(MET) = \text{Heating Voltage}$$

(B) VOLTAGE WAVEFORM

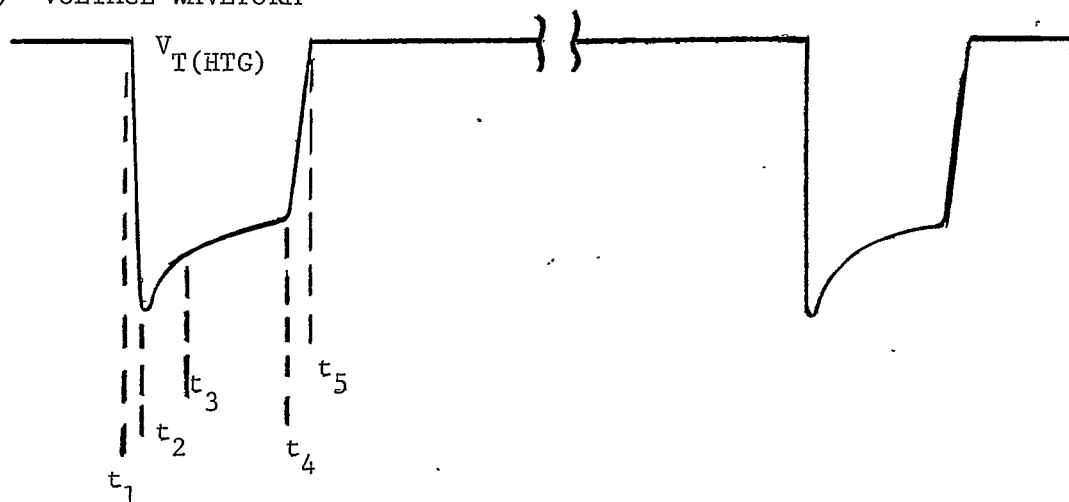


FIGURE 6.3.6-2 - CURRENT AND VOLTAGE WAVEFORMS  
DURING THERMAL RESISTANCE TEST

6.3.6.2.1.1 (continued)

The time  $t_3$  on the waveforms represents the shortest time after the removal of heating current that on-state voltage may be measured. Time  $t_3$  should be expected to be in the range of  $100^3$  to 200 microseconds for medium current (up to 150 A) device types, and up to 400 microseconds and higher for larger devices. For a particular device type, the time  $t_3$  is best found by performing the test at various power levels and noting the shortest time where the measured value of thermal resistance is essentially independent of the power dissipated. Power levels of 25% above and below the power corresponding to the specified heating current are recommended for this determination.

Since some active element cooling occurs between the time when the heating current is removed ( $t_1$ ) and time  $t_3$ , the thermal resistance value determined from a voltage measurement at  $t_3$  will be in error. It is therefore desirable to extrapolate the voltage waveform back to  $t_1$  from  $t_3$  based on the shape of the waveform from  $t_3$  to  $t_4$  where the waveform is a true representation of the junction temperature cooling curve.

Time constants of the device cooling curve are relatively long. Linear extrapolation of the actual cooling curve from time  $t_3$  back to time  $t_1$  results in little error and is recommended. Figure 6.3.6-3 illustrates the extrapolation.

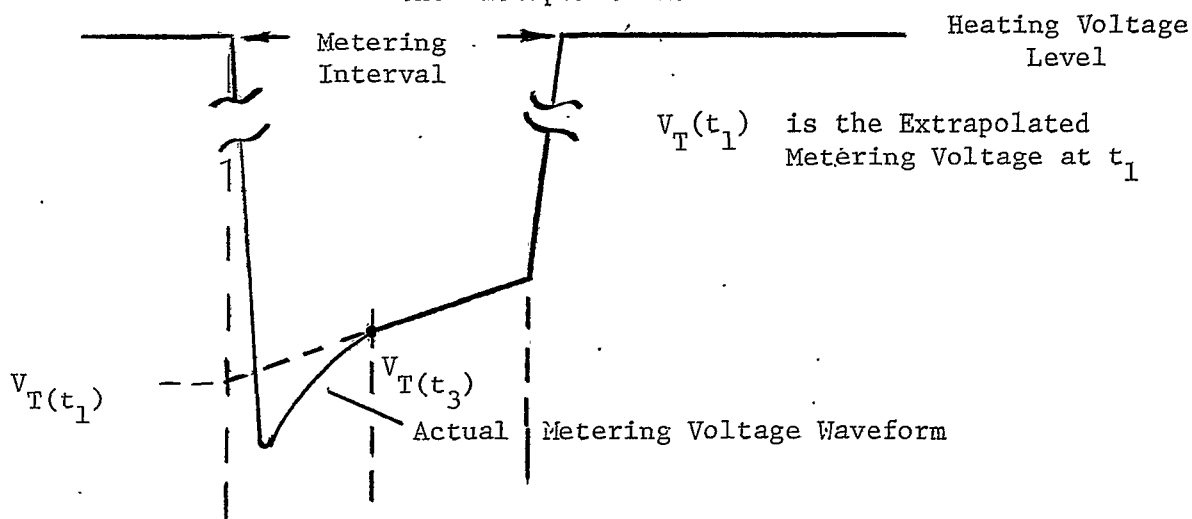


FIGURE 6.3.6-3 - ILLUSTRATION OF ON-STATE VOLTAGE WAVEFORM EXTRAPOLATION

6.3.6.2.1.1 (continued)

The heating current magnitude should be between one and two and one-half times the average current rating of the device. It must be applied for a time duration long enough for the thyristor active element and case to reach thermal equilibrium. The metering current magnitude should be low enough so that the resultant active element heating is negligible, but high enough above the device holding current so that effects due to irregularities in the thyristor low-level on-state characteristic are minimized. These effects, due to partial turn-on of the device junction area, can be extremely troublesome in making thermal resistance and transient thermal impedance measurements. A continuous gate current value helps reduce these effects and may be specified as a test condition. If no continuous gate current is to be used, the blank provided under "Test Conditions to be Specified" should be filled in with 0 mA dc.

In addition to recording the metering voltage waveform, the value of heating current  $I_{T(HTG)}$ , and the thyristor reference (case, lead or ambient) temperature, are to be recorded during Step 1.

Step 2 - Calibration Test

The power application test (Step 1) produces a value of on-state voltage at the metering current level (extrapolated back to time  $t_1$ ) which corresponds to the maximum virtual junction temperature attained. Step 2 consists of operating the test device with no significant power dissipation so that for all practical purposes, the thyristor virtual junction temperature and the reference temperature will be equal. The thyristor is operated at the same value of metering current as in Step 1. The on-state voltage is monitored while the thyristor is externally/heated on a temperature controlled block or in an oven until the measured value of on-state voltage equals the extrapolated value  $V_{T(t_1)}$  obtained previously. When the on-state voltage has stabilized, the thyristor reference temperature is recorded. This

6.3.6.2.1.2 (continued)

is the value  $T_{R1}$ . In the event that the determined value  $T_{R1}$  is not within 20% of rated junction temperature, which is a specified test condition, Step 1 must be repeated using a different heating current amplitude. However, since thermal resistance is not strongly dependent upon junction temperatures, the thermal resistance value computed may be used to compute a fairly accurate estimate for the second trial.

Control of the heating current through the device under test is accomplished by  $SCR_1$  and  $SCR_2$  (refer to Figure 4) which function as a flip-flop switching with a sufficient repetition rate to facilitate oscillographic observations. Current is carried by  $SCR_1$  only during the on-state voltage metering interval so this  $SCR$  may be considerably smaller than  $SCR_2$ . Capacitor  $C_1$ , which is charged by a lower current dc power supply, has the function of turning off  $SCR_2$  when  $SCR_1$  is triggered.

Unavoidable inductance in the heating current power supply and associated circuit wiring make it impossible to turn off the heating current abruptly without creating transient voltages which would interfere with the measurement of on-state voltage. To overcome this, a diverter circuit, consisting of rectifier diodes  $RD_1$  through  $RD_5$ , is included so that heating current is not interrupted by  $SCR_2$ , but simply finds a different path. The inductor  $L_1$  may be included to make certain that the heating current does not vary while it transfers from one path to the other. This inductor also serves to reduce, to a negligible amount, undesired flow to current from  $C_1$  through the device under test and the heating current power supply. The inductance in the diverter circuit should be kept low so that after  $SCR_1$  begins to conduct, all heating current will be diverted away from the device under test fast enough to allow the specified rate of on-state current decay to be achieved. In Figure 6.3.6-4 the portion of the circuit in which inductance must be carefully controlled is indicated by heavy lines.

### 6.3.6.2.1.2 Test Circuit

A basic circuit which may be used for testing the thyristor in Step 1 with high-level (heating) current present is shown in Figure 6.3.6-4. The active element of the device under test is heated by a direct current having an rms ripple content of 5 percent or less which is passed continuously through the device under test except for the metering periods. During the metering periods, the junction temperature is indicated by reducing the on-state current to the metering current value and measuring the on-state voltage. This circuit will produce the on-state current and voltage waveshapes shown in Figure 6.3.6-2. Variations of this circuit which produce the same waveforms are permissible.

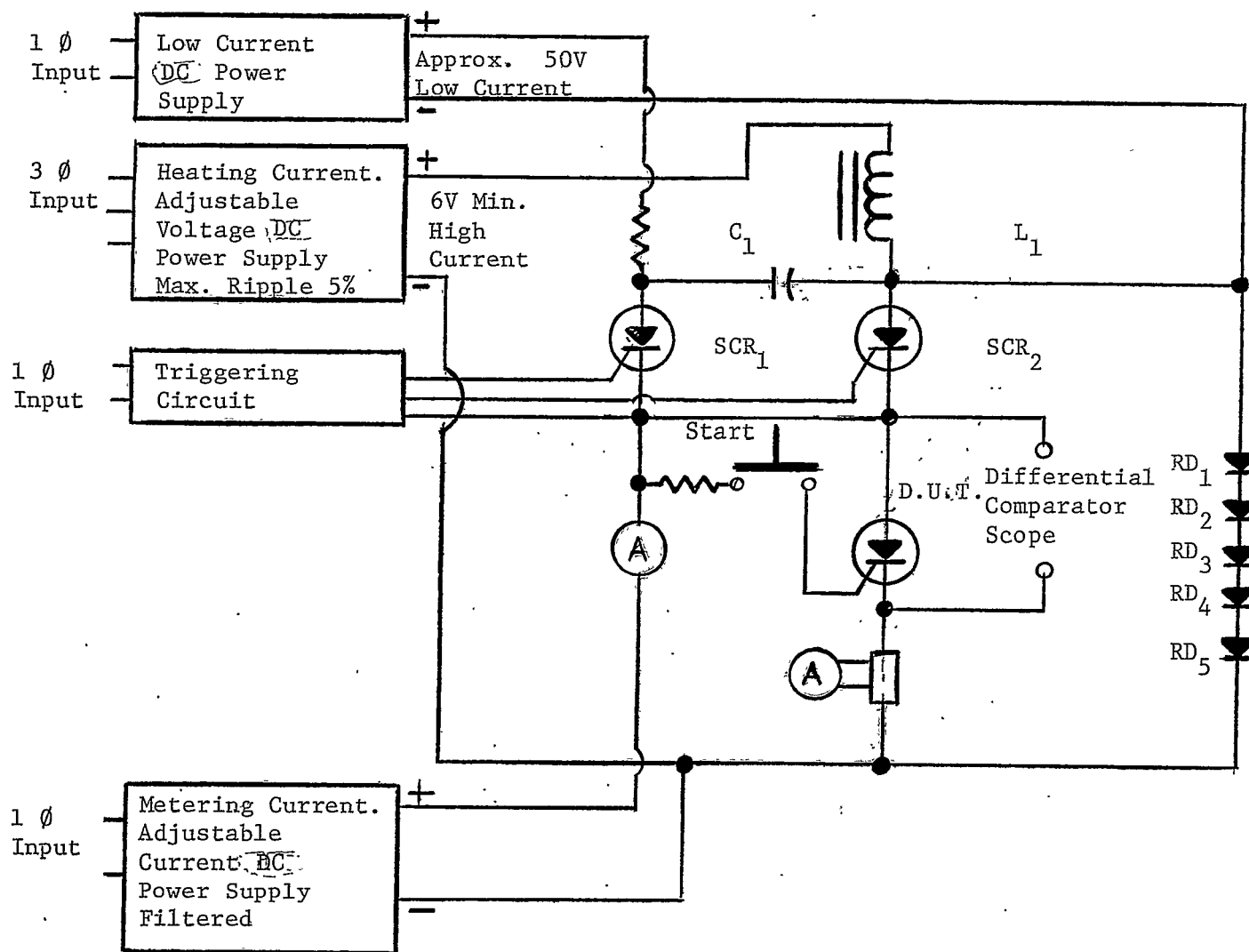


FIGURE 6.3.6-4 - THERMAL RESISTANCE TEST CIRCUIT

6.3.6.2.1.2 (continued)

In order to observe the on-state voltage of the test device during the metering current interval, the use of a differential comparator oscilloscope preamp is recommended. With care, this should allow magnification of the on-state voltage waveform during the metering current interval without distortion or zero shift being introduced due to the presence of the heating voltage waveform. Care must be taken to ensure that distortion or zero shift are not significant compared to the signal being measured. An oscilloscope camera is extremely useful for recording the waveform so that the photos can be used to obtain the data for the necessary extrapolation of the metering voltage waveform.

6.3.6.2.1.3 Test Conditions to be Specified

- (a) Metering On-State Current Amplitude \_\_\_\_\_ A dc.
- (b) Heating On-State Current Amplitude \_\_\_\_\_ A pk.
- (c) Heating On-State Current by Duty Factor 98% min.
- (d) Heating On-State Current Repetition Rate \_\_\_\_\_ Hz max
- (e) Rate of On-State Current Decay (See Note Below)  
(90% Point to Metering Current Level) \_\_\_\_\_ \*  
A/us min.
- (f) Measurement Time  $t_3$  (After Metering On-State  
Current Level is Reached) \_\_\_\_\_ us.
- (g) Total Heating Time Duration \_\_\_\_\_ s min.
- (h) External Reference Temperature Measurement  
Point \_\_\_\_\_.
- (j) Reference Temperature  $T_{R1}$  (Thyristor Maximum  
Rated  $T_J$ ) +0 -20% \_\_\_\_\_ °C.

\* NOTE: \_\_\_\_\_  
It may be necessary to take exception to this condition. This is particularly true for large thyristors which are operated at heating currents in excess of 100 amperes. When the exception is taken, the actual rate of decay must be specified.

#### 6.3.6.2.1.4 Characteristic to be Determined

Steady State Thermal Resistance,  $\theta_{JA}$  Junction to  
Specified Reference Point \_\_\_\_\_ C/W.

#### 6.3.6.3.1 Transient Thermal Impedance Test Methods

Measurement of transient thermal impedance by the heating pulse method is very similar to the measurement of thermal resistance, except that the heating current is applied as a single pulse. For the cooling method, a steady state condition is established under dc power conditions; upon power removal the on-state voltage with metering current applied is displayed on an oscilloscope and photographed.

##### 6.3.6.3.1.1 Heating Pulse Method Test Procedure

Considerations to be given to the metering current and proper extrapolation of the metering voltage waveforms are discussed in Section 6.3.6.2.1.1. Two distinct steps are utilized; a power application test and a calibration test.

##### Step 1- Power Application Test

The heating pulse of current is applied as a single pulse, approximately rectangular in shape and of specified width corresponding to the time value for which the transient thermal impedance is to be measured. Care must be taken, when applying heating current pulses, to avoid exceeding device non-repetitive surge current capabilities.

6.3.6.3.1.1 (continued)

The heating pulse current amplitude should be high enough to raise the test device virtual junction temperature to its maximum value  $\pm 0 - 20\%$ . Since the transient thermal impedance is lower for short pulse widths than for long pulse widths, a higher amplitude current pulse is required to heat the device junction when the pulse width is short. If the current pulse is so short that an excessive current amplitude would be required to attain rated junction temperature, external heating of the test device to an intermediate temperature may be employed.

For all but very short pulse widths it is generally necessary to employ an external heat dissipator to prevent appreciable device case temperature rise during the interval when power is applied. When an external heat dissipator is employed, the information regarding heat dissipator, mounting, and connection to the top terminal given in part 6.3.6.1.4 should be adhered to.

When an approximate value for the test device transient thermal impedance is known, equation (2) may be employed to calculate the approximate value of heating current required to raise the device virtual junction temperature to maximum rated value; otherwise, the required current magnitude must be arrived at by trial and error.

The measured value of heating current magnitude  $I_{T(HTG)}$ , heating voltage magnitude  $V_{T(HTG)}$ , and thyristor reference temperature  $T_{R2}$ , all must be recorded during Step 1. If the heating current waveform deviates much from a truly rectangular pulse, then graphical integration of the heating current and heating voltage waveform must be employed to determine the thyristor power dissipation.

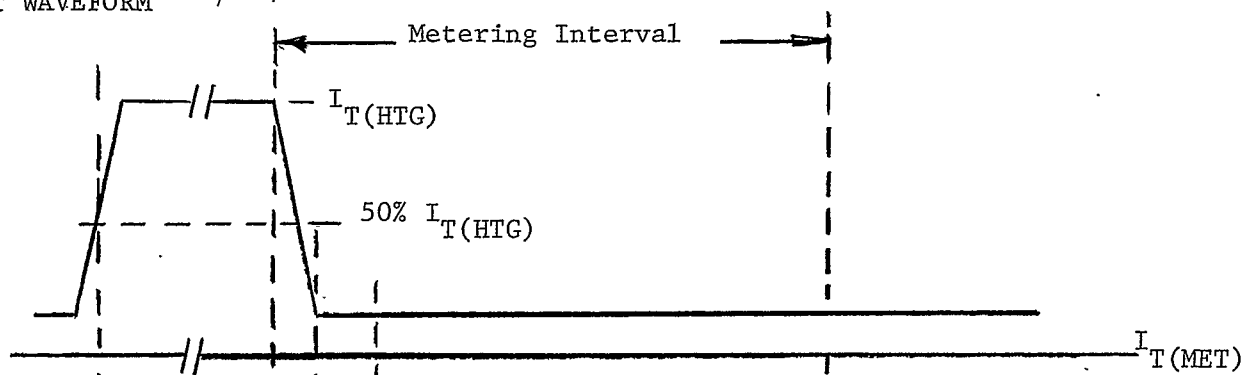
It must be recognized that thermocouple measuring system response time may cause some error on the measurement of  $T_{R2}$  for mid-range heating pulse widths. This may cause a discontinuity in a transient thermal impedance curve obtained for a wide range of pulse widths.



6.3.6.3.1.1 (continued)

As noted, Step 1 includes a metering voltage measurement to be used to determine device virtual junction temperature. It would be desirable to arrive at the device virtual junction temperature at the exact instant when heating current removal is initiated since the virtual junction temperature will be maximum at that time. However, this is not possible by direct measurement; because of transients which exist on the on-state voltage waveform, readout cannot commence until time  $t_3$ . It is necessary to use linear extrapolation from time  $t_3$  to  $t_1$  for most accurate results. See Figure 5 for an illustration of the waveforms and the extrapolation required. The discussion in part 6.3.6.2.1.1 provides further details.

a) CURRENT WAVEFORM



b) VOLTAGE WAVEFORM

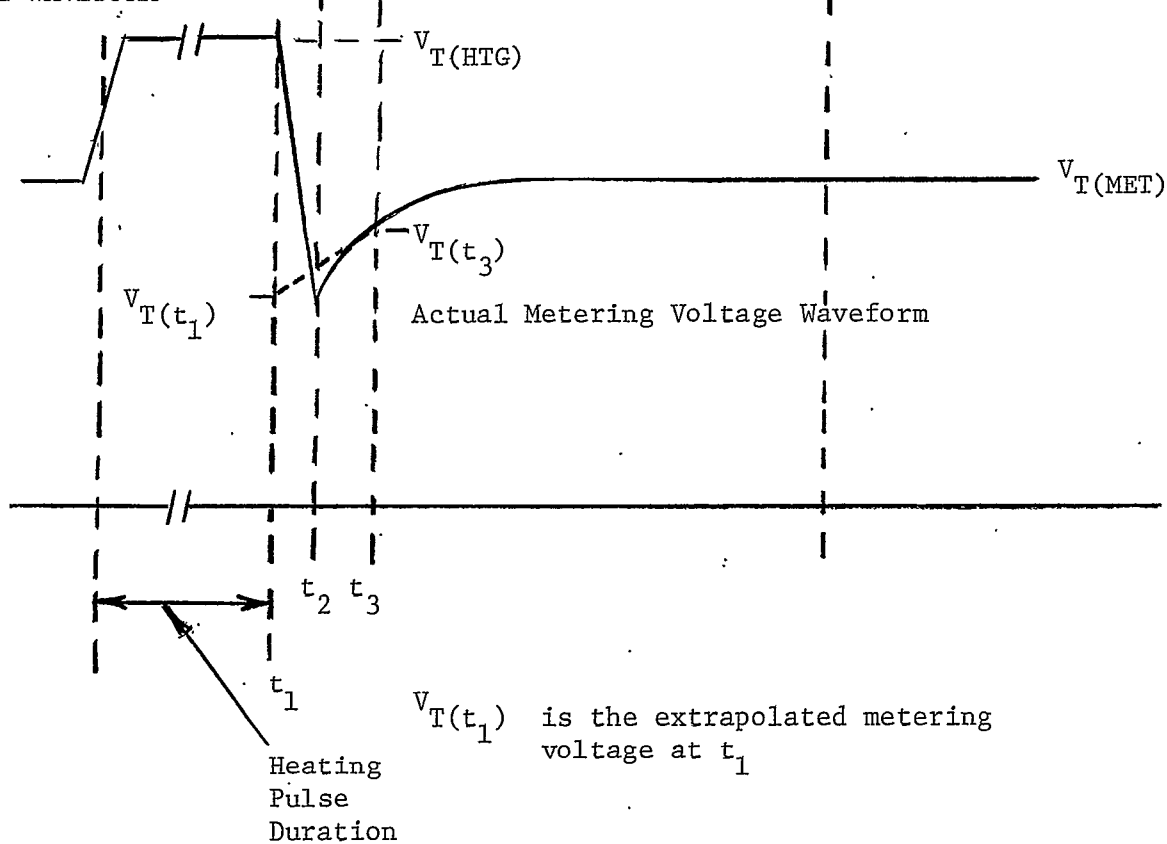


FIGURE 6.3.6-5 - CURRENT AND VOLTAGE WAVEFORM  
FOR TRANSIENT THERMAL IMPEDANCE TEST

6.3.6.3.1.1 (continued)

Step 2 - Calibration Test

The power application test (Step 1) produces a value of on-state voltage at the metering current level (extrapolated back to time  $t_1$ ) which corresponds to the maximum virtual junction temperature attained. Step 2 consists of operating the test device with no significant power dissipation so that for all practical purposes, the thyristor virtual junction temperature and the reference temperature, will be equal. The procedure is the same as given for the measurement of thermal resistance in Section 6.3.6.2.1.1 under "Step 2- Calibration Test". The value obtained is  $T_{R1}$ . In the event that the determined value of  $T_{R1}$  is not within the range 0 to -20% of rated junction temperature, which is a specified test condition, Step 1 must be repeated using a higher or lower heating current amplitude as may be required.

The transient thermal impedance can now be calculated from equation (2).

6.3.6.3.1.2 Cooling Curve Method Test Procedure

Two separate steps are also required for this method; a power application test and a calibration test.

Step 1 - Power Application Test

The heating current is applied as a continuous direct current for a time duration long enough to establish thermal equilibrium and then is interrupted. The magnitude of the heating current may range from the average current rating of the device up to two and one-half times this rating.

It is recommended that the transient thermal impedance test be performed so that the test device virtual junction temperature before the heating current is interrupted is in the range of maximum rated value +0 -20%. The size of the heat dissipator used must be chosen

6.3.6.3.1.2 (continued)

to accomplish this. The approximate reference temperature can be determined from the basic thermal resistance equation, equation (1).

The ambient temperature should be measured by means of a thermocouple mounted at a distance approximately 0.5 inch directly beneath the device under test.

The recommended heat dissipators and conductors to use with various types of devices when transient thermal impedance, junction-to-case, is to be measured are given in Section 6.3.6.1.4

After thermal equilibrium has been reached, the heating current magnitude  $I_{T(HTG)}$  and the corresponding heating voltage magnitude  $V_{T(HTG)}$  are recorded. The thyristor reference temperature  $T_{R2}$  must also be recorded. The heating current is then interrupted so that the test device only conducts the low-level metering current value. The rate of decay of heating current is an important test condition and must be specified. The on-stage voltage waveshape from the value when heating current is interrupted to the value at the time where the transient thermal impedance is to be measured, with metering current flowing, must be recorded as a function of time. This may be accomplished by photographing the oscilloscope trace of the voltage change. The trace will be similar to that shown in Figure 6.3.6-5 for Heating Pulse Method. The test may be repeated several times using a range of oscilloscope sweep rates to accurately record all portions of the voltage decay curve. Again, it is necessary to extrapolate the metering voltage back to time  $t_1$  to obtain the peak virtual junction temperature. The test device case temperature decay with time must also be recorded. Mounting the test device on a heat dissipator of large thermal capacity will minimize the change in DUT case temperature following the interruption of heating current.

6.3.6.3.1.2 (continued)

This information allows the virtual junction temperature of the test device to be determined for any specific time duration after interruption of the heating current. Information given in the previous paragraph entitled "Step 1 - Heating Pulse Method" regarding the metering current supply and choice of metering current magnitude applies for the cooling curve method also.

Step 2 - Calibration Test

Step 1 produces a curve versus time of low-level on-state voltage at the metering current level which must be converted by a calibration curve to junction temperature versus time. The calibration curve may be obtained by measuring on-state voltage at the metering current level (metering voltage) at various values of case or ambient temperature. Since there is no appreciable power dissipation at the metering current level, for all practical purposes the thyristor virtual junction temperature will be equal to the measured case, lead or ambient temperature. This temperature value is  $T_{R1}$ . The measurement should be made for at least three values  $T_{R1}$  with maximum value being equal to the rated operating junction temperature of the thyristor. A straight line drawn through the measured points is the desired graph. The general form of this graph is shown in Figure 6.3.6-6.

6.3.6.3.1.2 (continued)

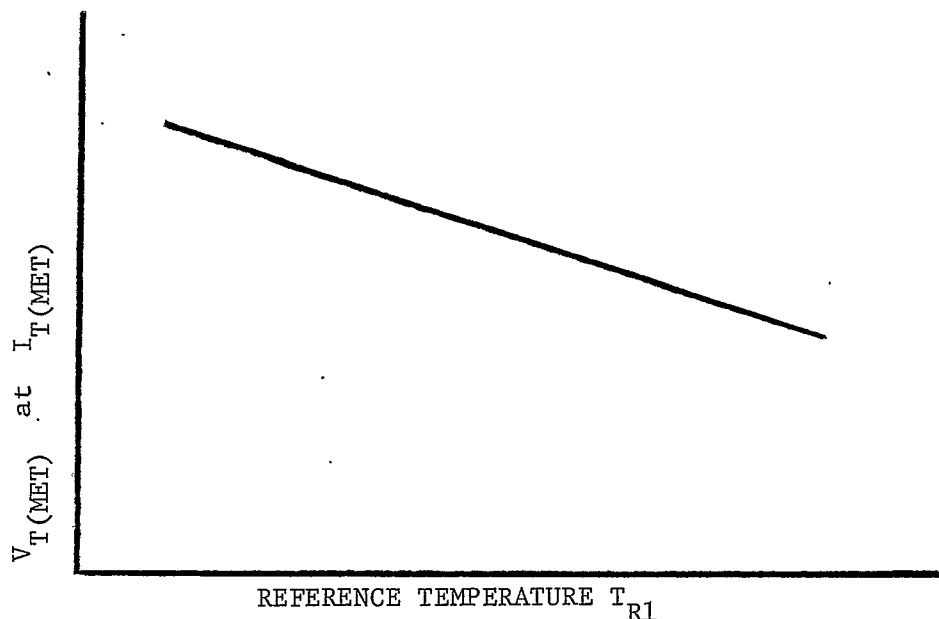


FIGURE 6.3.6-6 - THYRISTOR CALIBRATION CURVE

Transient thermal impedance at any time duration following the interruption of heating current can now be calculated converting the measured values of  $V_{T(MET)}$  on the photograph obtained in Step 1 to junction temperature using the calibration curve obtained as described above. The initial value of  $T_{R1}$  (at the instant of interruption of heating current) should be within 20% of thyristor maximum rated junction temperature; since this is a specified test condition. If the initial value of  $T_{R1}$  determined from the calibration curve does not fall within this range, then Step 1 must be repeated using either a different value of heating current or a different size of heat dissipator in order to satisfy the specified  $T_{R1}$  range condition.

A value of transient thermal impedance for the time interval being considered can now be obtained by using equation (2).  $T_{R2}$  is the reference temperature at the instant that heating power is removed. (If this temperature decays during the period when the junction is cooling, the measured junction temperature must be adjusted upward by the amount of reference temperature cooling that occurs.) However, since a cooling curve has been employed, the above calculated value must be subtracted from the thyristor steady-state thermal resistance to obtain a point on the transient thermal impedance curve (such as Figure 6.3.6-1) applicable to a power pulse of width equal to the time interval between the interruption of heating current and the point where the above temperature determination has been made.

#### 6.3.6.3.1.2 (continued)

For time values less than approximately one millisecond, the calculated values of transient thermal impedance may be in error because of device and equipment transients resulting from the interruption of the heating current. The point in time where the cooling curve starts to be a true representation of thyristor virtual junction cooling may be determined by employing heating currents which produce power levels 25% above and below the value which produces maximum rated junction temperature. This procedure and a method of extrapolation of the curve to the time of interruption of the heating current are further described in Step 1 for Thermal resistance.

#### 6.3.6.3.1.3 Test Circuits

A simplified basic test circuit for testing the thyristor in Step 1 is shown in Figure 6.3.6-7. The active element of the device under test is heated by direct current having a rms ripple content of 5% or less. The heating current is applied continuously when the cooling curve method is used for Step 1. When the heating pulse method is used for Step 1, the heating current must be interrupted after flowing for the time of interval for which the transient thermal impedance measurement is to be made (refer to Figure 6.3.6-5).

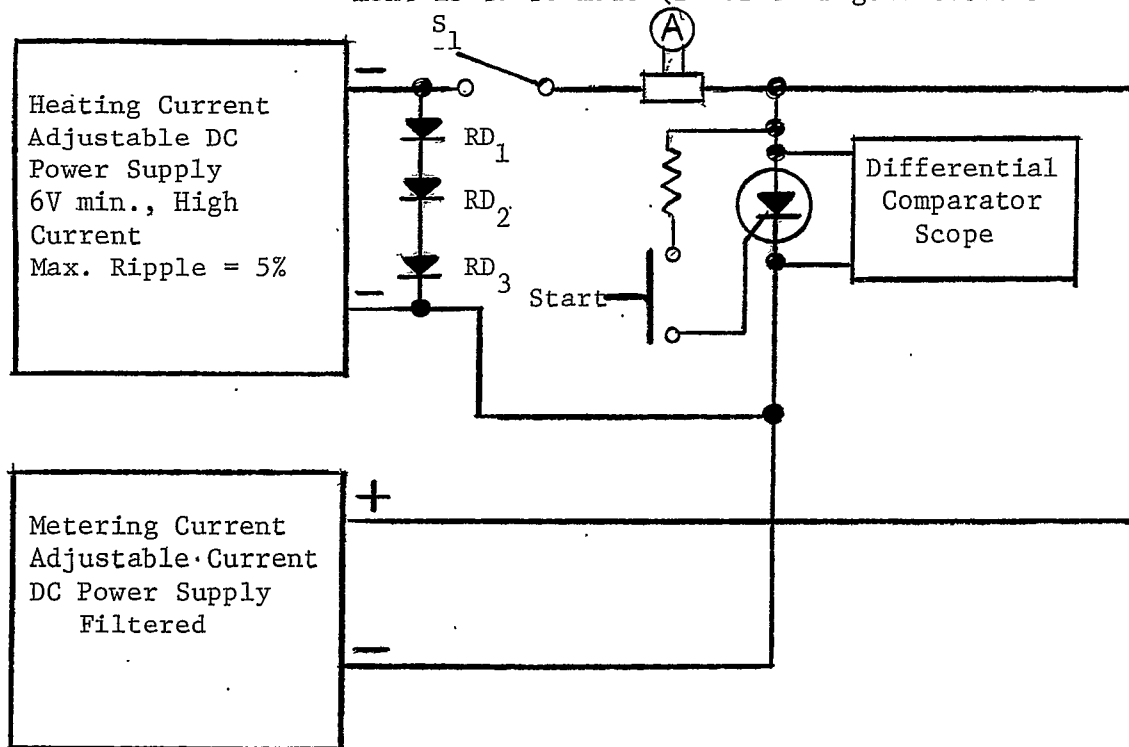


FIGURE 6.3.6-7 -BASIC TEST CIRCUIT FOR TRANSIENT THERMAL IMPEDANCE TEST METHOD

6.3.6.3.1.3 (continued)

The metering current supply remains connected throughout the heating current duration so that metering current is maintained after interruption of the heating current.

Control of the heating current amplitude is accomplished by adjustment of the supply voltage and/or variations of series resistance. Interruption of the heating current is made by opening switch  $S_1$ .  $S_1$  may be a manual switch when the cooling curve method is used. However, the switch must provide positive interruption and be free from contact bounce. The diverter circuit ( $RD_1$ ,  $RD_2$  and  $RD_3$ ) will assure clean interruption of the heating current through the DUT. An SCR, together with a suitable commutation circuit, may be used when the heating pulse is too short to be controlled by manual control. Thus, the basic circuit shown in Figure 4 for the steady-state thermal resistance test method may be used with a trigger circuit to control the SCR's and DUT suitable for single pulse operation. Variations of this circuit which will produce the specified test conditions are permissible. In order to achieve control of the rate of decay of heating current, care must be taken to control inductance in the heating current circuit.

In order to observe the on-state voltage of the test device during the metering current interval following heating current interruption, the use of the differential comparator oscilloscope pre-amp is recommended. With care, this should allow magnification of the on-state voltage waveform during the metering current interval without distortion or zero shift being introduced due to the presence of the heating voltage waveform. An oscilloscope camera is required to record the DUT on-state voltage during the time the junction of the DUT is cooling and to extrapolate the metering voltage back to the instant when the heating current was interrupted.



6.3.6.3.1.4 Test Conditions to be Specified

- (a) Method: (Heating or Cooling).
- (b) Metering On-State Current Amplitude \_\_\_\_\_ A dc.
- (c) Heating On-State Current Amplitude \_\_\_\_\_ A pk.
- (d) Heating On-State Current Pulse Width \_\_\_\_\_ s.
- (e) Rate of On-State Current Decay (See note below)  
(90% Point to Metering Current Level) \_\_\_\_\_ \* A/ $\mu$ s min.
- (f) Measurement Time  $t_3$  (After Metering On-State  
Current Level is reached) \_\_\_\_\_  $\mu$ s:
- (g) External Reference Temperature Measurement Point \_\_\_\_\_.
- (h) Temperature  $T_{R1}$  (Thyristor Maximum Rated  
Junction Temperature)  $\pm 0, -20\%$  \_\_\_\_\_  $^{\circ}\text{C}$ .
- (j) Temperature  $T_{R2}$  \_\_\_\_\_  $^{\circ}\text{C}$ .

\*NOTE: It may be necessary to take exception to this condition. This is particularly true for large thyristors which are operated at heating currents greater than 100 amperes. When exception is taken, the actual rate of decay used must be specified.

6.3.6.3.1.5 Characteristic to be Determined

Transient Thermal Impedance, Junction to  
Specified Reference Point, for Time Duration  
of \_\_\_\_\_ s. \_\_\_\_\_ C/W.

Time Duration Seconds							
Transient Thermal Impedance Deg. C per Watt							

### 6.3.7 Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors

#### 6.3.7.1 Test Description

This test applies to all bidirectional thyristors for both polarities of applied voltage.

The bidirectional thyristor, in its usual mode of operation, is required to switch to the opposite polarity off-state following current conduction in the on-state. In common 50/60 Hz or 400 Hz ac phase control applications utilizing sinusoidal voltage sources, this switching occurs each half cycle at the current zero point. This switching action is termed "commutation" and it is brought about by the reversal of the source voltage. The ability of the thyristor to maintain the off-state as this commutation voltage builds up in the opposite direction is determined by: (1) device operating temperature, (2) rate of reversal of current, (3) magnitude and time rate of application of commutation voltage.

This test method establishes the on-state current magnitude, duration, repetition rate, and rate of reversal; the device case temperature; and commutation voltage magnitude as test conditions and measures the critical rate of rise of the commutation voltage. The critical rate of rise of commutation voltage is the rate above which the device will not maintain the off-state but will conduct current in the opposite direction in the absence of a gate trigger signal. While this failure to switch to the off-state is not detrimental to the thyristor, it does result in loss of control of power to the load.

The voltage, current and temperature test conditions selected for this test are recommended to be the maximum registered values for the thyristor under test.

"Case temperature must be maintained within  $\pm 1^{\circ}\text{C}$  of the test condition value. A deviation beyond this temperature change will cause significant change in the test device commutating capability. The device under test may be triggered by means of any convenient trigger pulses of either polarity.

#### 6.3.7.2 Test Circuit

The test circuit to be used is shown in Fig. 6.3.7-2 and the test current and voltage waveforms are shown in Fig. 6.3.7-1.

6.3.7.2 (continued)

The power source for the test circuit is a 50/60 Hz or 400 Hz single phase sinewave supply which produces sinusoidal test current. The  $X/R$  for the entire test circuit shall be  $\geq 10$  so that the supply voltage and current are essentially in quadrature. The time rate of application of commutation voltage (test device off-state voltage) is essentially exponential and is determined by the setting of  $R_1$  and  $C_1$ . This voltage may be observed by means of an oscilloscope connected across the test device. The numerical value assigned to the  $dv/dt$  of the exponential voltage waveform is defined here as the slope of the straight line connecting the 10% and 63% points on the test voltage waveform. The 10% voltage point is used instead of zero because of the difficulty in determining the time point at which zero voltage occurs. The test voltage overshoot should be limited to 10% of the specified peak value of the test voltage.

In this test method the rate of reversal of test current ( $di/dt$ ) is quite circuit limited. Hence for thyristors with very good switching capability during commutation, the test device may maintain the off-state even when  $R_1$  and  $C_1$  are removed. In this case the  $dv/dt$  of the test voltage waveform is determined by the capacitance of the thyristor and distributed capacitance of other circuit components, particularly the reactor.

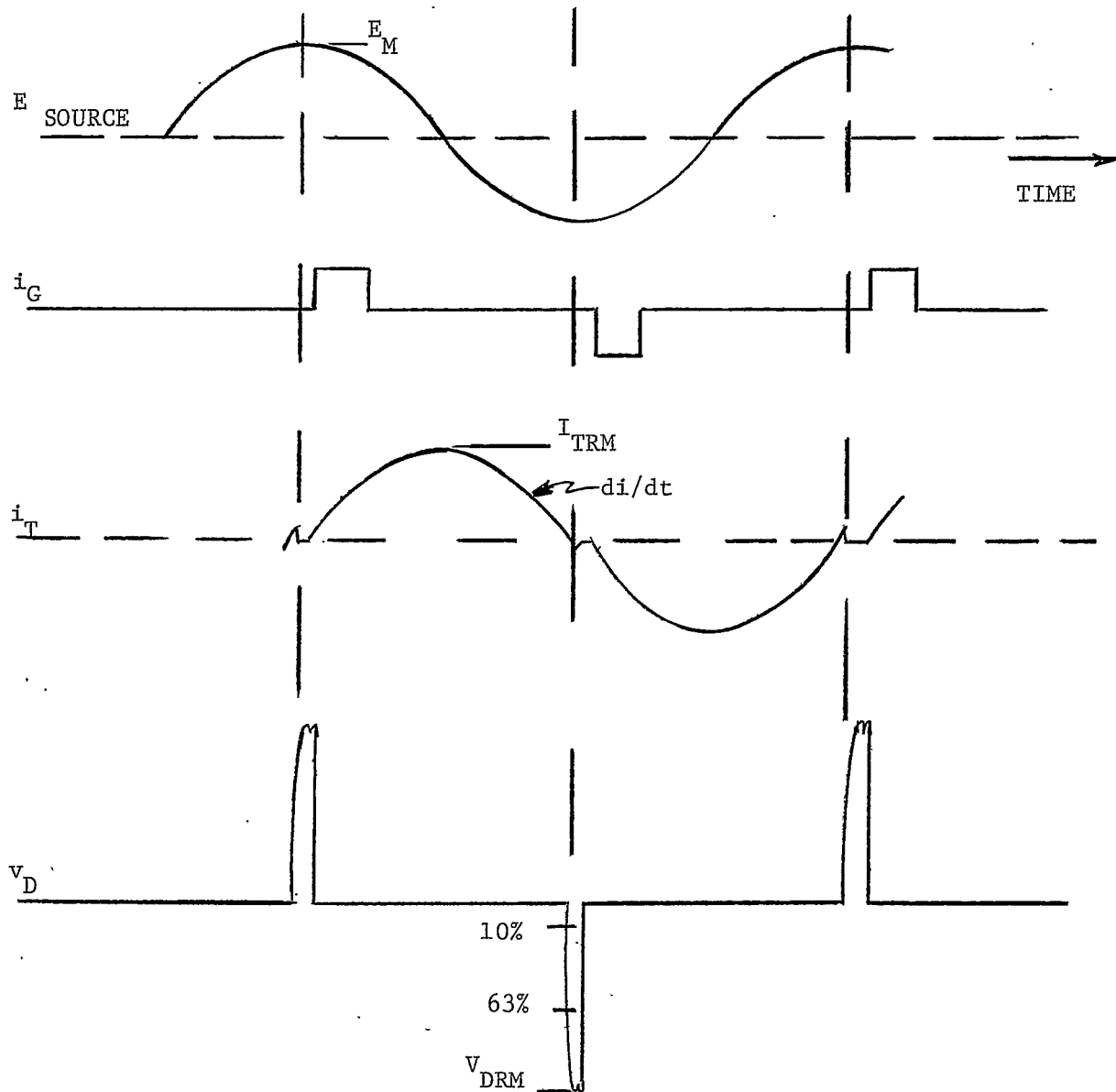


FIGURE 6.3.7-1 TEST WAVEFORMS

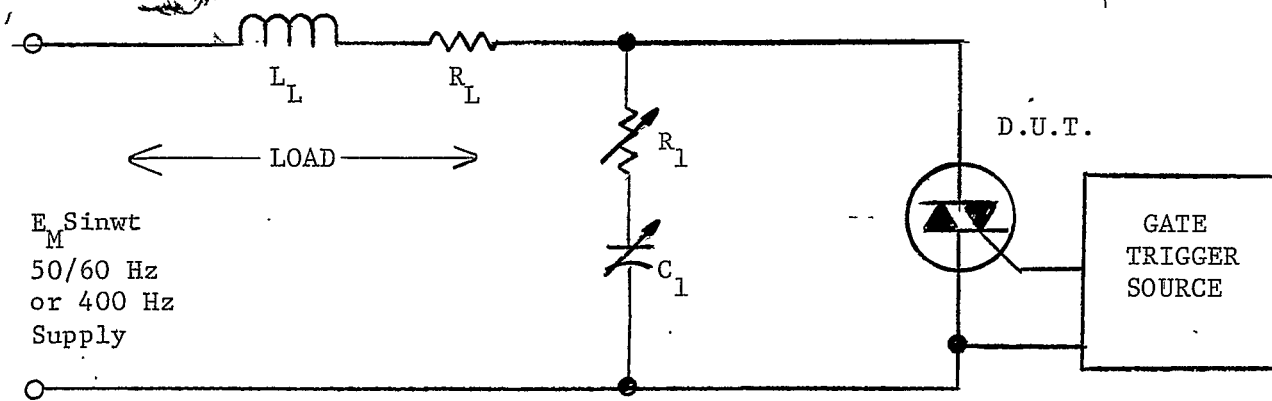


FIGURE 6.3.7-2 CRITICAL RATE OF RISE OF COMMUTATION VOLTAGE TEST CIRCUIT

### 6.3.7.3 Test Conditions To Be Specified

These specifications apply for each half cycle of the test voltage and current.

1. Frequency of Single Phase Sinusoidal AC Supply  
(50 or 60 Hz, or 400 Hz recommended) \_\_\_\_\_ Hz
2. Peak On-State Current ( $I_{TM} = \frac{E_M}{Z_L}$ ) \_\_\_\_\_ A
3. On-State Current Duration  
(90% of half cycle recommended) \_\_\_\_\_ ms
4. Rate of Reversal of On-State Current ( $di/dt$ )  
(The slope of the line connecting the 50% and 0%  $I_{TM}$  points;  $di/dt = (6 \frac{I_{TM}}{L} \times 10^{-6})$ ) \_\_\_\_\_ A/us
5. Peak Off-State Voltage ( $V_{DRM} \approx E_M$ ) \_\_\_\_\_ V
6. Off-State Voltage Duration  
(200 us min recommended) \_\_\_\_\_ us
7. Gate Bias Conditions (between current pulses)
 

Gate Source Voltage	_____	V
Gate Source Resistance	_____	ohms
or Gate Bias Resistance	_____	ohms
8. Case Temperature \_\_\_\_\_ °C

### 6.3.7.4 Characteristic To Be Measured

Critical Rate of Rise of Commutation Voltage  
(The slope of the line connecting the 10% and 63% test voltage points) \_\_\_\_\_ V/us

### 6.3.8 Reverse Recovery Characteristics for Thyristors Test Method

#### 6.3.8.1 Test Description

This test is applicable to all thyristors with the option of using a "soak current" to simulate a long current pulse width. It is particularly applicable to large area thyristors where the soak current eliminates the effects of incomplete current spreading. Use of a soak current is recommended for all thyristors rated over 25A unless it is desired to measure recovered charge under conditions simulating a particular narrow width pulse.

There are three characteristics of importance:

- (1) Reverse recovery time,  $t_{rr}$  ( $t_a + t_b$ )
- (2) Peak reverse recovery, current  $I_{RM(REC)}$
- (3) Recovered charge,  $Q_{R(REC)}$

The recovery current waveshape is classified as being one of two forms, soft or abrupt recovery. See the recovery current waveforms in Figure 6.3.8-3.

#### 6.3.8.2 Test Circuit

The circuit used for establishing these characteristics is shown in Figure 6.3.8-1. The circuit is designed to simulate the commutation duty encountered in power thyristor circuits. The test circuit waveform is shown in Figure 6.3.8-2.

There are essentially two main current loops,  $I_{TEST}$  and  $I_{SOAK}$ , which are shown in Figure 6.3.8.1.

The resistance of the loop containing  $L_2$  and  $C_2$  must be kept very small ( $R \ll 2\sqrt{L_2/C_2}$ , in order that the portion of the test current waveform generated by  $L_2$  and  $C_2$  will be essentially sinusoidal, possessing a width  $= \pi \sqrt{L_2 C_2}$ ,  $di/dt = V_2/L_2$  and a peak on-state current  $I_{TM} = V_2 \sqrt{L_2/C_2}$ .  $V_2$  is the peak voltage across capacitor  $C_2$ , and is to be made small as practicable to achieve the desired test current conditions.

6.3.8.2 (continued)

NOTE: This implies a large  $C_2$  and small  $L_2$ , which is consistent with the need to reduce transient voltages during the recovery period due to the value of  $L_2$ .

The loop containing  $C_1$  and  $L_1$  produces the "soak current" portion of the waveform. The resistance in this loop is not as critical as the  $C_2$  and  $L_2$  loop. With a somewhat overdamped  $RL_1C_1$ , a very satisfactory "soak current" is applied by triggering the device under test and SCR1. If no "soak current" is required, then only SCR2 and the device under test are triggered.

The purpose of the "soak current" is to simulate a trapezoidal current waveform. Specifically, it is used to provide sufficient current (magnitude and duration) to eliminate the effects of incomplete spreading in the device under test. The "soak current" magnitude and duration should also be limited to prohibit excessive junction heating of the device under test.

The termination of the "soak current" is determined by the triggering of SCR2. The voltage  $V_2$  must be greater than  $V_1$  so that SCR1 will be commutated off by triggering SCR2. The amplitude of the "soak current" is specified at  $t_1$  (see figure 6.3.8-2) to assure that the "soak current" does not drop below the value required to maintain full area conduction of the device under test.

The two most important test current conditions are its rate of reversal ( $di_R/dt$ ) and its magnitude.  $C_2$ ,  $L_2$ ,  $V_2$  and  $t_p$  are adjusted to achieve the desired test current  $di/dt$  and magnitude while at the same time keeping  $V_2$  time  $t_{rr}$ , of the test device so that the  $di_R/dt$  will be essentially linear and of the same value before and after current reversal.  $di/dt$  may be calculated from the peak current  $I_{TM}$ , and the time from the peak of the current pulse to current zero,  $t_c$ , by means of this relationship.



#### 6.3.8.2 (continued)

$$di_R/dt = \frac{\pi I_{TM}}{2t_c} = \frac{\pi I_{TM}}{t_p}$$

The inductance of the current viewing resistor must be extremely low, e.g.,  $\leq 0.01$  uhenry. The oscilloscope used to view the current must possess sufficient bandwidth to faithfully reproduce the true current waveform. If certain types of test devices recover too abruptly (Figure 6.3.8-3, a current oscillation may appear on the oscilloscope following device recovery. This may be reduced by using a lower inductance current viewing resistor and by using a properly terminated oscilloscope connection cable. This oscillation, however, does not have any bearing or effect on the test results. (A current transformer or a current probe may also be used to observe the current through the device under test.)

Rectifier Diode D2 and its circuit branch should provide a very low inductance path around SCR2, if the reverse recovery time of SCR2 is shorter than that of the device under test.

#### 6.3.8.3 Waveform of Recovery Current and Definition of Recovery Time

Thyristors can possess two broad types of recovery characteristics. After the test current reaches its peak reverse value  $I_{RM(REC)}$  it may immediately or a short time later decrease very abruptly (abrupt recovery) or it may decrease slowly and smoothly to its steady state reverse blocking value (soft recovery).

Figure 6.3.8-3 illustrates four types of recovery current waveforms. Figure 6.3.8-3a is a typical soft recovery, and Figures 6.3.8-3b, and 6.3.8-3d illustrate types of abrupt recovery, since high  $di_{(REC)}/dt$  is present.

The fairly rapid change of current ( $di_{(REC)}/dt$ ) from peak recovery current ( $I_{RM(REC)}$ ) towards its steady state reverse blocking value causes a transient reverse voltage (produced by circuit inductance) to appear across the device under test.

#### 6.3.8.3 (continued)

The magnitude of this voltage may exceed the rating of the device under test. Although it is recommended that an RC snubber not be used, one may have to be connected across the device under test and current viewing resistor to reduce the transient voltage magnitude.

Recovery time for thyristors is defined as  $t_{rr} = t_a + t_b$  (see Figures 6.3.8-2 and 6.3.8-3). For a thyristor possessing "soft" recovery characteristics  $t_a$  is measured from the instant of current reversal to the instant the current reaches its peak reverse value  $I_{RM(REC)}$  and  $t_b$  is measured from  $I_{RM(REC)}$  to the instant the straight line connecting  $I_{RM(REC)}$  and  $0.25 I_{RM(REC)}$  intercepts the zero current axis.

Recovery time for devices possessing the "abrupt" recovery characteristics shown in Figures 6.3.8-3b and 6.3.8-3c is defined in the same manner except  $t_b$  is measured to the instant the test current waveform apparently intercepts the zero current axis. For the abrupt recovery waveform of 6.3.8-3d  $t_b$  is defined in the same manner as soft recovery. Note that the shape of the recovery characteristics can be fairly well determined if the value of  $t_b$  is compared to that of  $t_a$ . It is for this reason that the recovery characterization is done in this manner. (Note that for go-no-go reverse recovery testing, limit points  $I_{RM(REC)}$  and  $0.25 I_{RM(REC)}$  should be based upon the registered  $I_{RM(REC)}$  maximum value.)

#### 6.3.8.4 Recovered Charge

The recovered charge is essentially represented by the area under the reverse current-time curve. An approximate value of the recovered charge can be calculated by the expression:

$$Q_{R(REC)} = 1/2 \left[ t_{rr} \cdot I_{RM(REC)} \right]$$

6.3.8.4 (continued)

These measurements may be made manually or electronically. If an electronic process is employed (to measure  $Q_{R(REC)}$ ) it is more expedient to define the end point of  $t_r$  by an actual current amplitude, rather than by extrapolation. In this case the recovery current at which the end point is established shall be specified as  $I_{R(REC)}$ , and shall be equal to 10% of  $I_{RM(REC)}$  unless a smaller percentage is specified.

6.3.8.5 Test Conditions to be Specified

- (a) Case Temperature = \_\_\_\_\_ °C
- (b) Test Repetition Rate = \_\_\_\_\_ Hz
- (c) Peak On-State Test Current,  $I_{TM}$  = \_\_\_\_\_ A
- (d) Rate of Reverse of On-State Test Current,  $di_r/dt$  = \_\_\_\_\_ A/us  
(measured as it crosses the current axis).
- (e) Test Current Pulse Width,  $t_p \geq$  \_\_\_\_\_ us  
(Duty cycle must be  $\leq 1\%$ )
- (f) Thermal Resistance of Minimum Heat Dissipator upon which Test Device is mounted,  
 $R_{\theta SA} =$  \_\_\_\_\_ °C/W
- (g) Duration of Soak Current ( $t_1 - t_o$ ) = \_\_\_\_\_ us (min)  
\_\_\_\_\_ us (max).
- (h) Soak Current at  $t_1 =$  \_\_\_\_\_ A(min) \_\_\_\_\_ A(max) \_\_\_\_\_ uF(max)
- (j) Value of RC Snubber,  $R =$  \_\_\_\_\_ ohms  
(if required)  $C =$  \_\_\_\_\_ uF
- (k) Gate Bias Conditions
  - 1. Gate Source Voltage = \_\_\_\_\_ V
  - 2. Gate Source Resistance = \_\_\_\_\_ ohms

6.3.8.6 Characteristics to be Measured

(a) Reverse Recovery Time (Defined as  $t_{rr} = t_a + t_b$ )  $t_a =$  \_\_\_\_\_  $\mu s$

$t_b =$  \_\_\_\_\_  $\mu s$

$t_{rr} =$  \_\_\_\_\_  $\mu s$

(b) Reverse Recovery Current,  $I_{RM(REC)} =$  \_\_\_\_\_ A

(c) Form of Recovery Current Waveform (Abrupt or Soft) = \_\_\_\_\_

(d) Recovered Charge,  $Q_{R(REC)} =$  \_\_\_\_\_  $\mu C$

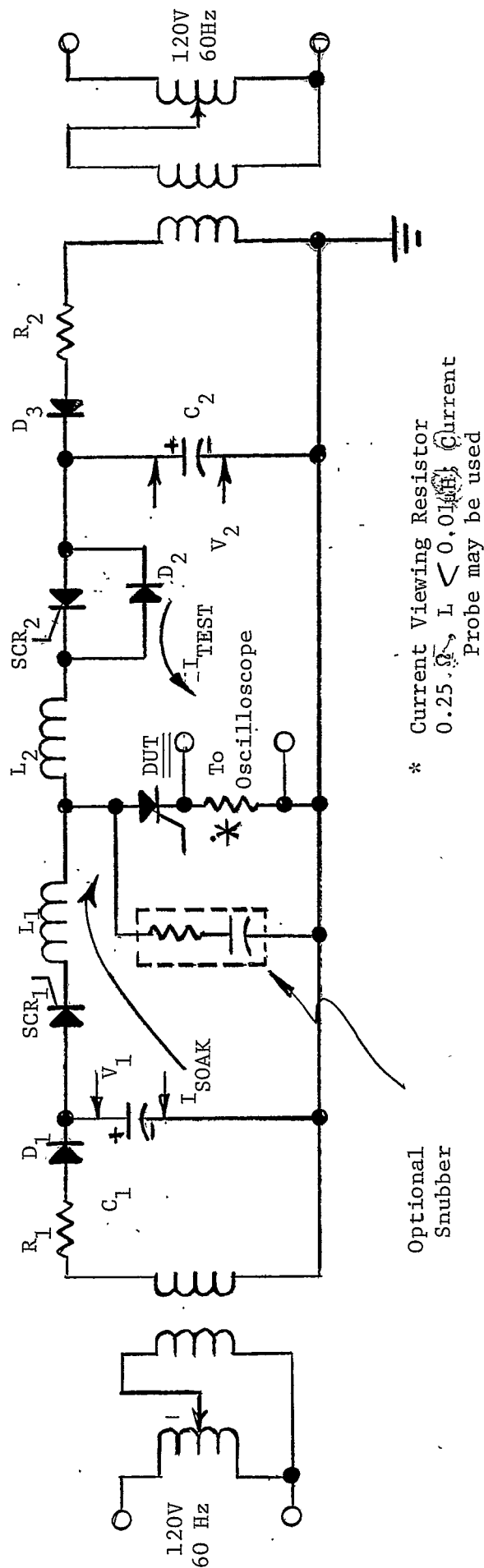
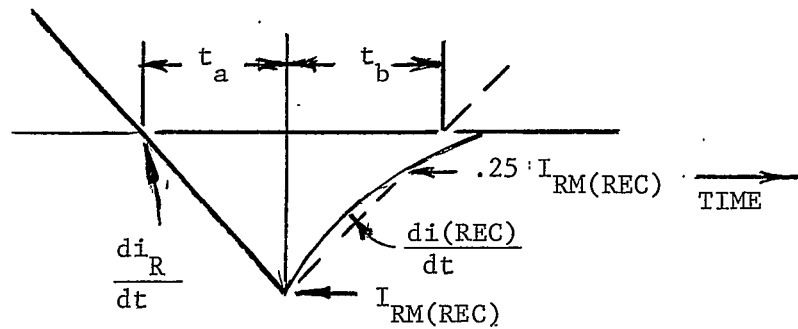
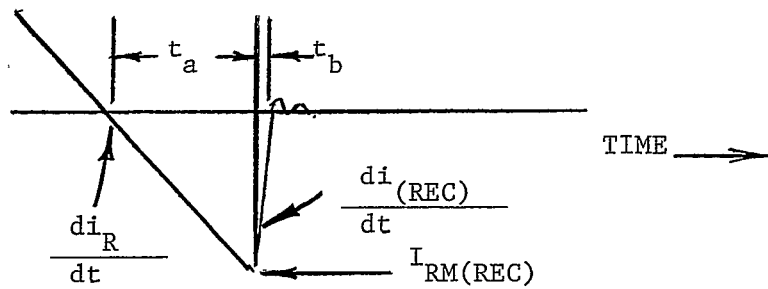


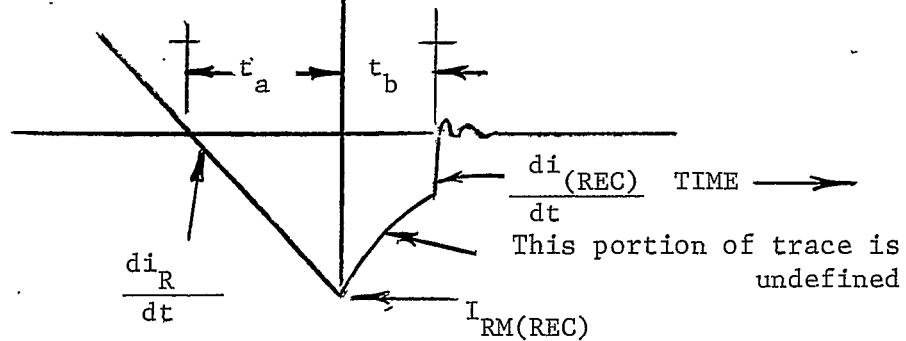
FIGURE 6.3.8-1 - Circuit for measuring Reverse Recovery Characteristics for Thyristors



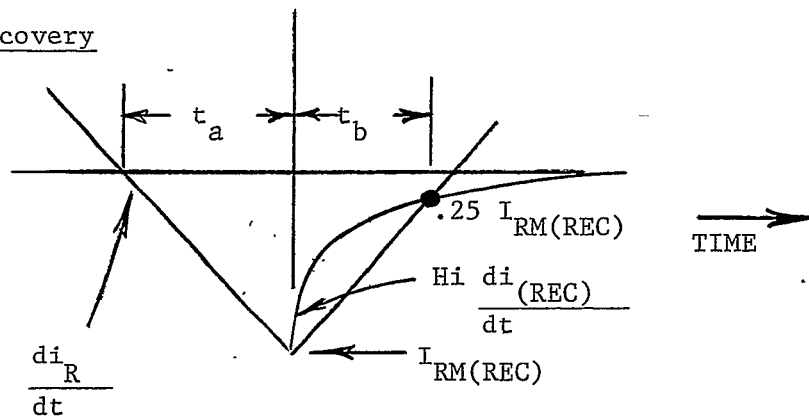
a) Soft Recovery



b) Abrupt Recovery



c) Abrupt Recovery



d) Abrupt Recovery

FIGURE 6.3.8-3: Reverse Recovery Current Waveform for Various Types of Thyristors

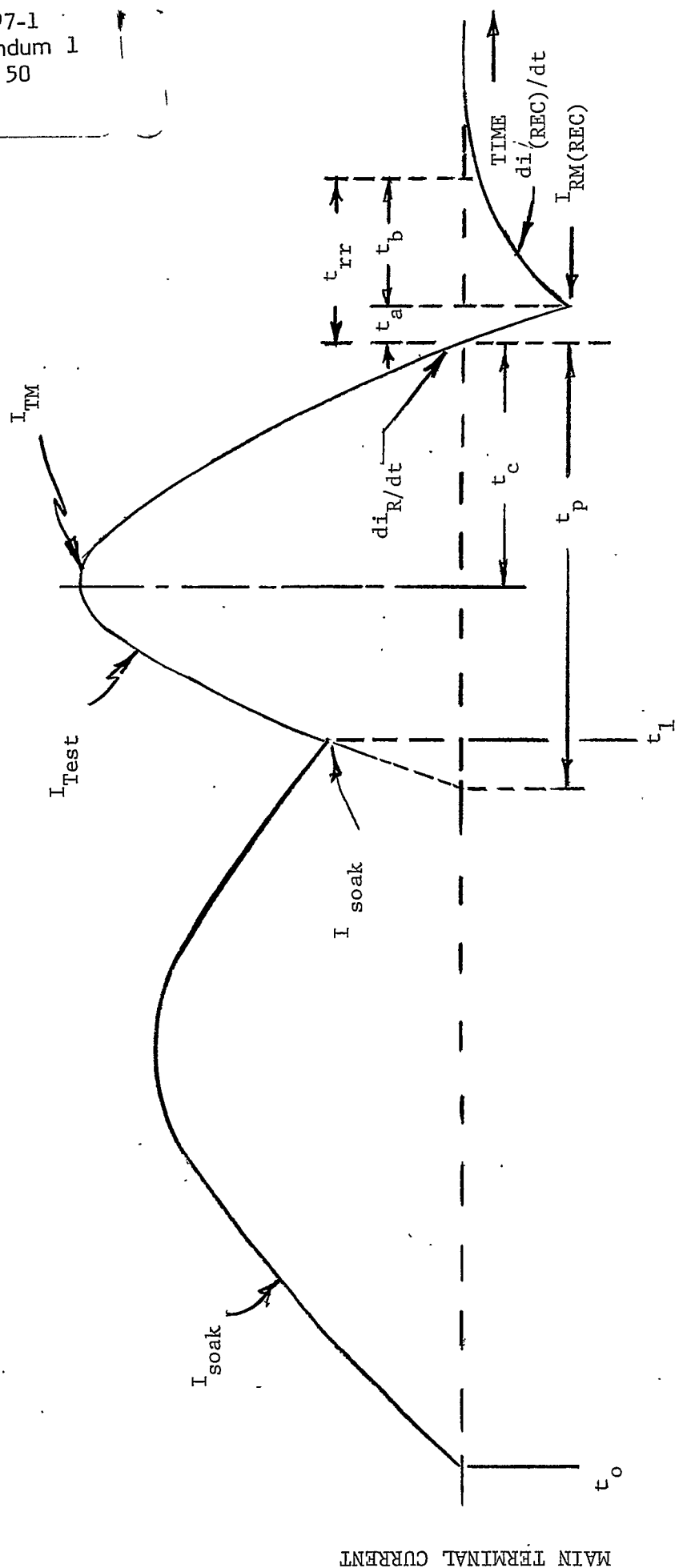


FIGURE 6.3.8-2: Test Circuit Waveform for Measuring Reverse Recovery Characteristics of Thyristors

### 6.3.9 Suppressible Surge Current Characteristic

#### 6.3.9.1 Test Description

This test is used to establish suppressible surge current characteristics for reverse blocking triode thyristors. Unlike the non-repetitive 60 Hz Surge Current Rating  $I_{TSM}$ , this test requires the device to maintain off-state voltage blocking capability after the surge current interval. Primarily intended for SCR's in high power systems. This type of characteristic is needed in applications where the thyristor is subjected to random short circuit loads and then is required to sustain off-state voltage immediately following circuit voltage reversal.

As in most surge or fault situations the junction temperature of the device may exceed (during the surge current interval) the maximum allowable steady junction temperature. In this suppressible surge current characteristic the critical parameter is the device junction temperature at the time off-state voltage is reapplied. Depending on the junction temperature at this critical time other device characteristics may be a primary factor in determining the suppressible surge current characteristic. These characteristics are gate trigger current and voltage, turn-off-time, leakage current, and  $dv/dt$ .

The junction temperature at the critical time the off-state voltage is reapplied will be primarily determined by the case temperature, the magnitude of the steady state load current and the magnitude, shape and duration of the surge current. The time between the end of the surge current and the application of reapplied off-state voltage will also influence this temperature.

It is possible, therefore, to have an almost infinite number of combinations of case temperatures, load current, surge current and reapplied off-state voltage conditions. To simplify the test and in the interest of interchangeability of devices of various manufacturers, the test conditions to be specified in 6.3.3. have been assigned specific values wherever possible.



#### 6.3.9.1 (continued)

The test device is brought up to the desired steady-state case temperature by means of a heated test fixture. The time between on-state current surges should be long enough to permit the device virtual junction temperature to return to its original thermal equilibrium value. The device under test should be triggered with sufficient gate drive to ensure full turn on.

#### 6.3.9.2 Test Circuit

This test circuit to be used is shown in Figure 6.3.9-1 and voltage and current waveforms are shown in Figure 6.3.9-2.

The desired repetitive peak 60Hz sine wave reverse and off-state voltages are applied to the test device. The surge current pulse and reapplied reverse and off-state voltages are controlled by SCR's 1, 2 and 3 in the test circuit. Sufficient delays should be provided in the triggering of SCR3 to assure that SCR1 is fully off.

The time from the end of the on-state surge current pulse ( $t_1$ ) to the beginning of the off-state voltage waveform ( $t_2$ ) shall be specified. This time ( $t_2 - t_1$ ) can be varied in rough steps by proper selection of two phases of a three phase incoming line. The times that can be so obtained are approximately 2.2, 5.0 and 7.7 ms with 7.7 ms being the value obtained when both input transformers are connected to the same phase; the value of 7.7 ms is recommended. Circuit B (Figure 6.3.9-1 may be used to obtain continuous adjustment).

The reapplied off-state voltage should be observed on an oscilloscope to determine that the device blocks the first half cycle of off-state voltage following the surge current. Failure of the device to block the reapplied off-state voltage following the current surge indicates the suppressible surge current limit has been exceeded.

6.3.9.3 Test Conditions To Be Specified

1. Surge Current. Pulse Width ( $t_1 - t_0$ ) \_\_\_\_\_ A  
(asymmetric half sine wave, 8.3 to 9.5 ms)
2. Time from end of the on-state surge current pulse to the beginning of the off-state waveform ( $t_2 - t_1$ ) \_\_\_\_\_ ms  
(a value of 7.7 ms is recommended)
3. Magnitude of peak reapplied off-state voltage \_\_\_\_\_ V  
(Standard values of 100%, 80%, 67%, 50% and 33% of maximum rated  $V_{DRM}$  with 67% being the most common)
4. Case temperature prior to surge current \_\_\_\_\_ °C  
(a value 25°C lower than maximum rated is recommended)
5. Gate bias conditions (following the surge current)  
Gate source voltage \_\_\_\_\_ V  
Gate source resistance \_\_\_\_\_ ohms  
or Gate Bias resistance \_\_\_\_\_ ohms  
(Recommended values are 0.0 volts and 100 ohms)
6. Device mounting  
Minimum mounting force \_\_\_\_\_ lb  
or minimum mounting torque \_\_\_\_\_ lb - in
7. Time between surge current pulses. \_\_\_\_\_ seconds  
(minimum time is 1 minute, unless thermal equilibrium is achieved in a shorter time)

6.3.4 Characteristic to be measured

Peak on-state surge current magnitude \_\_\_\_\_ A

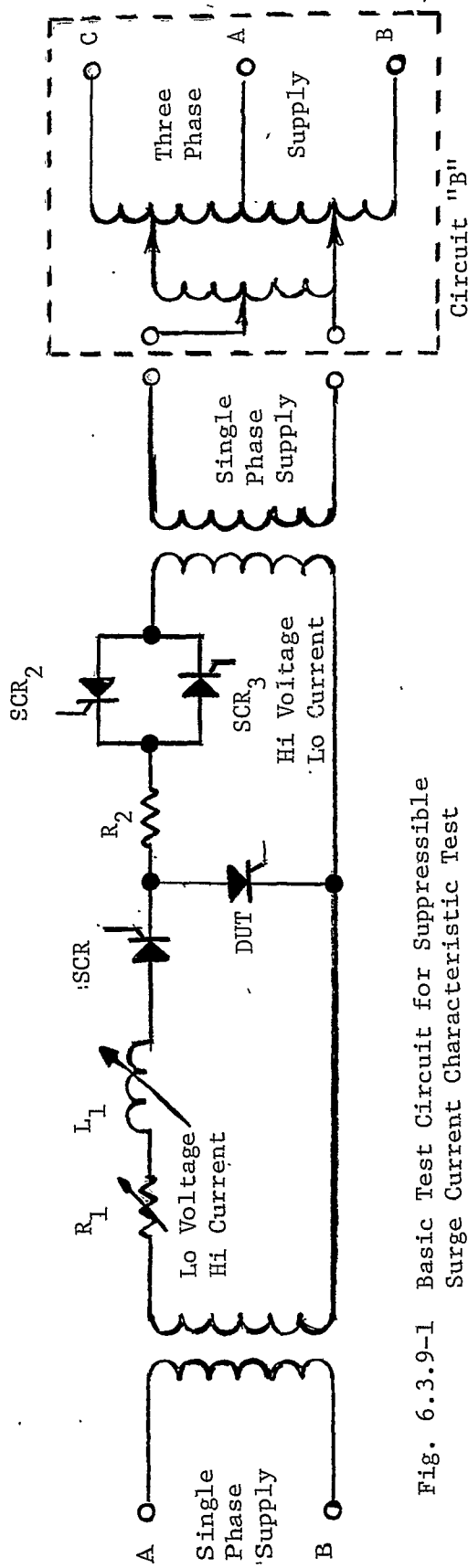
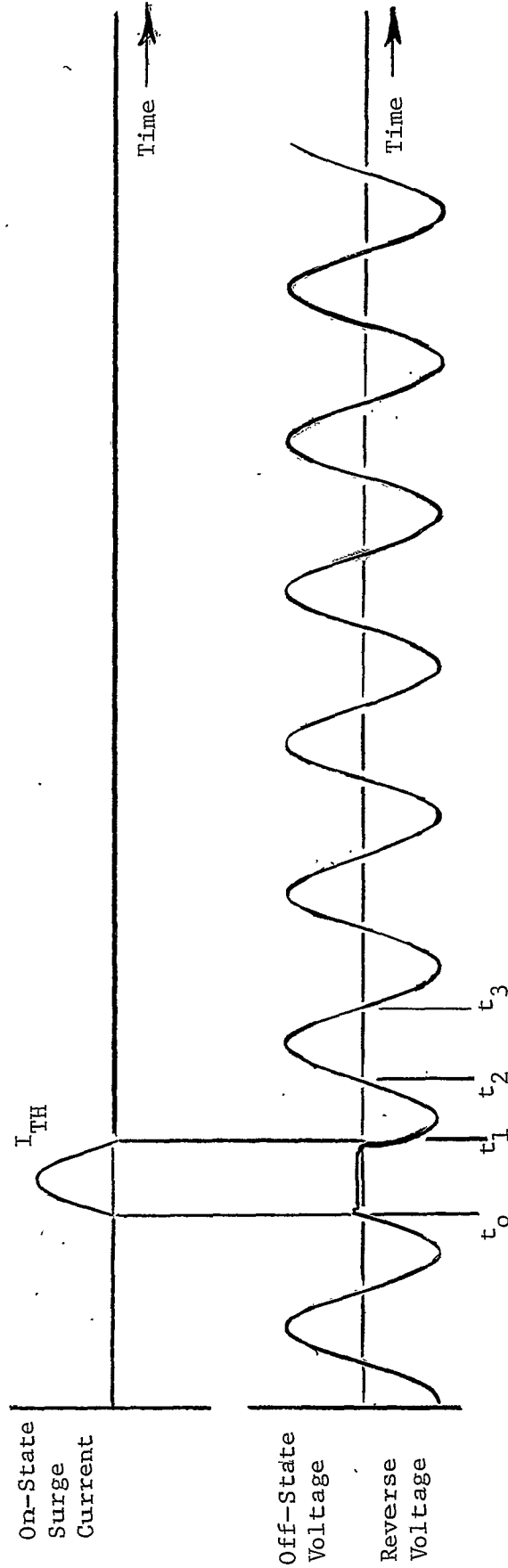


Fig. 6.3.9-1 Basic Test Circuit for Suppressible Surge Current Characteristic Test



$t_1 - t_0$  Duration of on-state surge current pulse.

$t_2 - t_1$  Time between end of surge current pulse and start of reapplied off-state voltage.

$t_3 - t_2$  Duration of reapplied off-state voltage.

FIG. 6.3.9-2 Current and Voltage Waveforms Applied to the Device Under Test

PART 7  
USER'S GUIDE  
INDEX

- 7.1 Introduction
- 7.2 Thyristor Safety Considerations
- 7.3 Voltage Considerations
  - 7.3.1 Basis for and Comparison of Thyristor Voltage Ratings
    - 7.3.1.1 Repetitive Peak Reverse Voltage
    - 7.3.1.2 Non-Repetitive Peak Reverse Voltage
    - 7.3.1.3 Repetitive Off-State Voltage
    - 7.3.1.4 Peak Principal Voltage
  - 7.3.2 Overvoltage
  - 7.3.3 Series Operation
- 7.4 Current Considerations
  - 7.4.1 Maximum Operating Junction Temperature
  - 7.4.2 Junction Heat Generation
  - \*7.4.3 Thermal Resistance
  - 7.4.4 Steady State Current Ratings
  - 7.4.5 Overload Current Ratings
  - 7.4.6 Parallel Operation
- 7.5 Triggering
  - 7.5.1 Gate Triggering of Triode Thyristors
  - 7.5.2 Triggering of Diode Thyristors
- \*7.6 Switching
  - 7.6.1 Turn-On of Triode Thyristors
  - 7.6.2 Rate-Of-Rise of On-State Current in Triode Thyristors
  - 7.6.3 Turn-On Dissipation
  - 7.6.4 Reverse Recovery

7.6.5 Turn-Off

\*7.6.6 Commutation Ability (Bidirectional Thyristors)

7.7 Fundamental Thyristor Circuits

\*7.8 Heat Dissipator Considerations

\*7.8.1 General

\*7.8.2 Handling Considerations

\*7.8.3 Contact Surfaces

\*7.8.4 Mounting Torque (Stud Type)

\*7.8.5 Clamping Pressure (Disc Type)

7.9 Temperature Measurements

7.9.1 General

7.9.2 Ambient Temperature

7.9.3 Thyristor Temperatures

7.9.4 Temperature Measurements Involving Thyristors Mounted  
on Heat Dissipators

7.10 Thyristor Failure Modes

7.10.1 General

7.10.2 Catastrophic Failure

7.10.3 Degradation Failures

7.11 Radio Frequency Interference

7.12 Simple Measurements in Trouble Shooting

7.12.1 Off-State and Reverse Blocking Voltage Checks

7.12.2 Gate Trigger Check

### 7.4.3 Thermal Resistance

A measure of the effectiveness with which a semiconductor device is able to get rid of heat is called thermal resistance. The lower the device thermal resistance figure, the lower the junction temperature rise for a given conduction current and resulting junction power generation. When thermal resistance is specified, the beginning and end of the thermal path must be clearly indicated. The common thyristor device thermal resistance specification is the value from the junction to a particular point on the case. For stud-mounted thyristors, this point is generally the center of one of the hex flats. (Refer to paragraph 7.9.3.3).

The heat flow associated with thyristor junction-to-case thermal resistance may be considered unidirectional. For the direct conduction current situation, Fourier's steady state heat flow relations are analogous to Ohm's steady state direct current flow relations.

$$\begin{array}{c} \text{Ohm's Law} \\ I = \frac{\Delta V}{R} \end{array}$$

$$\begin{array}{c} \text{Fourier's Law} \\ P = \frac{\Delta T_{JC}}{R_{\theta JC}} \end{array}$$

I = Direct current flow through R in Amperes

R = Electrical resistance in Ohms

$\Delta V$  = Voltage difference across R in Volts

P = Power on heat flow in Watts

$R_{\theta JC}$  = Thermal resistance from junction to case in  $^{\circ}\text{C/W}$

$\Delta T_{JC}$  = Temperature difference across  $R_{\theta JC}$  in degrees C.

When the heat flow (and device current flow) is periodic or pulsating, the small thermal capacitance (heat storage capability) of the silicon crystal in the thyristor causes the junction temperature to rise and fall with the pulsating power generation. Thus, if the thyristor dc or effective junction-to-case thermal resistance is multiplied by the average power generated by a pulsating current, the result will be the average junction temperature rise above the case temperature. To find the peak junction temperature in this case, the thyristor transient thermal impedance characteristic must be used in a power superposition calculation. The reader is referred to the literature where this procedure is adequately covered. Now, it is possible to answer the question

#### 7.4.3 (continued)

as to which instantaneous junction temperature is used by the manufacturer to establish the device maximum operating junction temperature rating. For this rating, different manufacturers may use any one of the following:

- a. Peak junction temperature - That is, the highest instantaneous junction temperature produced by periodic conduction current waveforms.
- b. Average junction temperature - That is, the average junction temperature produced by periodic conduction current waveforms.
- c. The instantaneous temperature at the conclusion of the conduction current- That is, the junction temperature at the instant the blocking voltage is applied.

The most common thermal resistance specification published by thyristor manufacturers is the dc (sometimes called effective) thermal resistance parameter. This parameter is measured by using dc device heating current which produces dc device power dissipation. Often a thermal parameter called apparent thermal resistance is also published. This parameter applies only for a specified periodic conduction current waveform. It is useful in that it can eliminate the use of transient thermal impedance characteristic in determining the thyristor case to junction temperature rise for that current waveform. This is done by multiplying the average power produced by a particular magnitude of the periodic current waveform in question by its corresponding apparent thermal resistance value. In the case of SCR's used in phase control applications, commonly published apparent thermal resistance parameters are for 60 Hz single phase half wave ( $180^\circ$ ), three phase full wave ( $120^\circ$ ), and six phase half wave ( $60^\circ$ ). In the case of the triac, the published apparent thermal resistance parameter usually applies for a 60 Hz full sine wave current waveform.

If a semiconductor manufacturer does not publish apparent thermal resistance parameters, they can be calculated from the following information:

- (1) Average power  $P_{T(AV)}$  vs current magnitude  $I_{T(AV)}$  for the periodic current waveform in question.
- (2) Maximum current rating  $I_{T(AV)}$ , vs case temperature ( $T_C$ ) for the same current waveform.
- (3) Maximum operating junction temperature  $T_{J(MAX)}$  rating for the device:

$$\text{Apparent thermal resistance} = \frac{T_{J(MAX)} - T_C}{P_{T(AV)}}$$

#### 7.4.3 (continued)

Note that by using the apparent thermal resistance parameter and a current vs power curve, it is a simple matter to determine the operating junction temperature of a thyristor for any selected case temperature and conduction current magnitude.

### 7.6 Switching

#### General

There are four distinct switching characteristics which are of interest with thyristors: (1) turn on, (2) reverse recovery, (3) turn off ability (one type of off-state recovery) and (4) commutation ability (a second type of off-state recovery applicable to bidirectional thyristors only.) As phenomena, these can be considered separately, though in many applications, such as high frequency or pulse circuits, the four effects become inter-related.

#### 7.6.1 Turn-On of Triode Thyristors

In applications such as radar pulse modulators, power supply crowbars, or control and alarm circuits, where the speed-of-response of the thyristor becomes a measure of performance, the gate controlled turn-on time ( $t_{gt}$ ) may be reduced significantly by overdriving the gate with signals larger than the dc gate current which will just accomplish triggering (as specified by the manufacturer). Curves relating  $t_{gt}$  to the magnitude of the gate signal are generally available. Overdriving the gate by two to ten times the minimum signal level will usually accomplish most of the reduction in turn-on time possible and will reduce the variation in  $t_{gt}$  between thyristors of the same type and between subsequent pulses applied to the same unit (jitter). Increasing temperature and voltage will generally reduce the delay time interval, though not by an appreciable amount.

The rise-time portion of the total turn-on interval is affected strongly by the circuit conditions during turn-on. In higher voltage, lower current, noninductive circuits, the dynamic impedance of the thyristor is a small percentage of overall circuit impedance and the rise of current to the 90% point occurs more rapidly.

#### 7.6.2 Rate-of-Rise of On-State Current in Triode Thyristors

At the end of the delay and rise time periods, as defined by the gate-controlled turn-on time, the thyristor will be in conduction through only a portion of its total available conduction area. A further interval is required for the current to spread from the initial area turned on which is close to the gate, to the rest of the conduction area. During this time, the rate-of-rise of the on-state current should be kept within the critical rate of rise of on-state current ( $di/dt$ ) rating of the device so that excessive localized heating of that portion of area which is in conduction will not be encountered. The  $di/dt$  ratings may be either repetitive



#### 7.6.2 (continued)

or non-repetitive types and will therefore apply respectively to continuous operation or infrequent overload situations.

The use of a fast rising gate pulse of large magnitude will usually improve the thyristor's  $di/dt$  capability by increasing the area initially entering conduction. It should be emphasized that the specified conditions of the  $di/dt$  rating should include a gate current magnitude which generally will represent some overdriving of the gate beyond the minimum requirements for dc triggering. Turn on of the thyristor at other gate currents or by other mechanisms such as exceeding the breakover voltage or by  $dv/dt$  may result in a different  $di/dt$  capability.

After an appreciable on-state current is reached, the gate signal has little influence on the rate of current spreading to the remaining conduction area. In cases where  $di/dt$  stresses exceed the device capability, linear or self-saturating reactors may be inserted in the circuit to lower  $di/dt$  or to delay the onset of the bulk of the load current until device current spreading is nearly complete.

Among the circuits which are very likely to produce  $di/dt$  problems are those where capacitors are being discharged. The capacitor discharge may be the prime function of the thyristor or it may be a secondary consideration, such as the discharge of a capacitor used for transient overvoltage protection. In any case,  $di/dt$  must be controlled by adequate impedance in the discharge loop.

However, even in such low frequency circuits as 60 Hz phase control applications, situations can arise where  $di/dt$  is beyond device capability. For example, in SCR circuits feeding inductive dc loads, the rate of current commutation from one phase to another in three phase systems is inversely proportional to the ac system impedance. Where such thyristor circuits are directly connected to an ac system of low short-circuit impedance,  $di/dt$  stresses in the thyristor when turning on should be considered. This kind of problem may be encountered more often in large ac/dc power conversion equipments since  $di/dt$  capability is not generally proportional to the current rating of the thyristor.

#### 7.6.3 Turn-On Dissipation

Apart from the limitations of  $di/dt$  ratings, the power dissipation during turn-on may become a limiting factor in the high frequency performance of a thyristor. As switching frequency increases, turn-on losses may become large compared to on-state losses. This may necessitate operation at lower than rated 60 Hz current or reduction of turn-on losses by control of  $di/dt$ .

#### 7.6.4 Reverse Recovery

In switching from the on-state to reverse blocking, a large initial reverse current will flow through a reverse blocking thyristor. The rate of rise of this current is determined only by the external circuit. After a short interval, less than a few microseconds, the thyristor will become able to block reverse voltage and the reverse current will decay to the normal blocking level. The magnitude of the reverse recovery current may be large enough to warrant consideration in determining the rating of other circuit components which supply this current, particularly with respect to turn-on dissipation in another thyristor. In addition, the decay of the peak reverse recovery current may be abrupt enough to generate large transient overvoltages in inductive circuit components feeding this current. Such overvoltages may be controlled in a variety of ways, the simplest of which is often the use of capacitor in parallel with the thyristor of sufficient size to accept the stored inductive energy from the circuit without excessive voltage rise. This capacitor should have a resistor in series to limit turn-on dissipation in the thyristor when it is switched on again.

#### 7.6.5 Turn-Off

The turn-off time of a thyristor describes the minimum interval of time after the end of conduction of on-state current before off-state voltage can be reapplied without the device turning on. If adequate turn-off time is not provided and the thyristor inadvertently switches to the on-state when off-state voltage is reapplied, this is not in itself damaging to the device. The circuit action resulting from failure to turn off may produce undesirable effects, however, such as high dc fault currents which may exceed the device capability. In dc switching circuits such as inverters and switching regulators, the magnitude of the turn-off time which must be provided for the thyristor directly influences the upper limit of operating frequency, and the size of the commutating components which provide for turn-off.

Factors causing an increase in turn-off time are: high junction temperature, high forward current prior to turn-off, rapid reduction of forward conduction to zero, limited reverse recovery current, low reverse blocking voltage, a fast rate of rise of voltage from reverse blocking to off-state, and a large magnitude of off-state voltage. Thyristors which are optimized for fast turn-off are available and are generally less sensitive to the above conditions, than are normal designs. It should be noted that turn-on dissipation may influence turn-off time in two ways. First, the rate of decay of turn-on induced hot spot temperatures in silicon material is generally slow compared to the interval between turn-on and turn-off in circuits above a few kilohertz. Therefore, some portions of the device may

#### 7.6.5 (continued)

not turn off under high frequency operation. Secondly, turn-on dissipation may, at high frequencies, increase the average power loss appreciably and therefore raise the average junction temperature, leading to increased device turn-off time.

Conservative design practice should provide some safety factor in circuit turn-off interval beyond the device turn-off time rating to allow for abnormal circuit operating conditions, such as greater than normal supply voltage and load magnitude, high current during start-up conditions, etc. It should be recognized that the numerous circuit influences on turn-off time may differ in an operating circuit from those used in manufacturers' specification of turn-off time.

#### 7.6.6 Commutation Ability (Bidirectional Thyristors)

The bidirectional thyristor, in its usual mode of operation, is required to switch to the opposite polarity off-state following current conduction in the on-state. This switching action is termed "commutation" and it is brought about by the reversal of the source voltage. The ability of the thyristor to maintain the off-state as this commutation voltage builds up in the opposite direction is strongly influenced by:

1. Device operating temperature
2. Magnitude and rate of reversal of principal current
3. Magnitude and time rate of application of commutation voltage

The critical rate of application of commutation voltage is the characteristic which defines the commutation ability of a bidirectional thyristor. When testing for this characteristic the case temperature must be maintained within  $\pm 1^{\circ}\text{C}$  of the required value. A deviation beyond this range will cause significant change in the test device commutation ability. Increasing temperature will cause the commutation ability to decrease.

The magnitude and rate of reversal of principal current must be defined and controlled to achieve accurate results. An increase in the rate of reversal of current will cause a decrease in the commutation ability.

The commutation ability is somewhat dependent on the magnitude of the commutation voltage. The higher the rate of application of voltage the more dependent it becomes on the magnitude of the commutation voltage. An increase in the magnitude of the commutation voltage will cause a decrease in the commutation ability.

## 7.8 Heat dissipator Considerations

### 7.8.1 General

In order to achieve the full current carrying capability of stud, base-mounted, or disc type thyristors, it is required that they be attached to heat dissipators (heat sinks). In general, disc type devices are cooled by pressing a heat dissipator or heat exchanger against each mounting surface, although single sided cooling may be used of the resulting reduced efficiency of heat removal is acceptable. The heat dissipator(s) must be securely clamped parallel to the mounting surface(s) of the semiconductor device. Exceptions to this are those thyristors which are lead-mounted or possess large integral heat dissipators. These types of devices have their current ratings referred to ambient temperature. Of course, these types of thyristors may also be assigned current ratings based upon their case temperatures.

### 7.8.2 Handling Considerations

Care must be used in handling and mounting Power Thyristor devices to avoid causing nicks, scratches or other deformations which reduce contact area between the two mounting surfaces, as these can impede the flow of heat to the heat dissipator(s), resulting in an excessive temperature rise.

### 7.8.3 Contact Surfaces

#### 7.8.3.1 Contact Surface Preparation

To produce a reliable low electrical and thermal resistance between the mating surfaces it is necessary that they may be free of all foreign material, oxides and films. Freshly machined surfaces are generally free of these contaminants if used immediately. Note that an oxide film forms on bare aluminum in a matter of seconds. Copper oxidizes more slowly.

As a precautionary measure, all mating surfaces, and particularly aluminum, should be used immediately after machining. If they are stored, a cleaning operation before use is a good practice. A satisfactory cleaning technique is to polish the mounting areas with No. 400-600 grit paper, followed by a solvent rinse. No. 000 steel wool can be used to polish contact areas but care must be taken to remove steel particles from insulators so that device flash-over will not occur.

#### 7.8.3.1 (continued)

Many aluminum heat dissipators are black anodized for appearance, durability, performance and economy; however, anodizing forms a film which is an electrical and thermal insulator. This anodic film should be removed from the mounting area. Another aluminum protective finish is irridite, or chromate acid dip, which offers low resistance because of its them surface. But, for optimum performance, it must be cleaned of oils and films that collect during the manufacture and storage of the heat dissipators. For ecocomy, paint is sometimes used. When this finish is used, removal from mounting areas is mandatory, because of its high thermal and electrical resistance.

#### 7.8.3.2 Contact Surface Finish

The contact surface of each heat dissipator must be flat and have as smooth a surface finish as the mating surface of the semiconductor device. In general, a total indicator reading (TIR) of less than .0015 inch should be observed over any area which is to come in contact with one of the device mounting surfaces. The surface finish on the heat dissipator contact surface should be in the range of 30 to 60 microinches. (0.8 to 1.5 micrometers)  $\mu\text{m}$  (04 millimeters). Machining of the mounting surface(s) often is required to achieve these conditions.

#### 7.8.3.3 Lubrication of Contact Surfaces

Even though all the procedures previously listed are followed, it is still possible to have air voids between mating surfaces; these interfere with the flow of heat between such surfaces. To reduce the thermal resistance introduced at these mating surfaces it is recommended that they be coated with a thermal joint compound. Such a compound also has the desirable property of keeping moisture away from the mating surfaces, and hence inhibiting corrosion, particularly if the plating has been damaged. These compounds may contain deoxidizers for the purpose of further retarding corrosion. Bare metal surfaces may be plated as another means of inhibiting corrosion.

Joint compounds are often a formulation of fine metallic particles in a petroleum or silicone base which maintains a grease-like consistency in spite of the passage of time and elevated temperatures. The joint compound should be applied in a very thin layer to avoid an increase in the interface thermal resistance. This coating may be applied with a spatula or lintless brush. Another method is to place a predetermined minimal amount of the compound at or around the center of the mounting area, and then during mounting of the semiconductor device rotate it to force the joint compound to spread out all over the contact area. (Note: Bulk greases may impair

#### 7.8.3.3 (continued)

heat transfer as the bulk material may interfere with intimate contact of the mating surfaces.) If reassembly of a disc semiconductor to a heat dissipator is required where a metal bearing thermal compound was used, the device and heat dissipator surfaces should be refinished. The semiconductor device manufacturer may be consulted for more information on thermal joint compounds and their application.

#### 7.8.4 Mounting Torque (Stud Types)

Good thermal contact between the base of the thyristor and the heat dissipator requires adequate pressure between the two contact surfaces. This is produced by torque on the threads of the device. However, a torque beyond a certain point no longer improves the thermal contact and may mechanically stress the semiconductor crystal and associated materials inside the housing. For this reason, precise adherence to the manufacturer's torque recommendation is necessary, and this should be verified by using a torque wrench. The torques specified for lubricated and non-lubricated stud threads may be different; the device manufacturer's recommendation on mounting torque should be followed. When a device with a copper stud is mounted through a clearance hole in an aluminum heat sink, the unequal temperature coefficients of aluminum and copper can cause the mounting to gradually loosen as the assembly is cycled through temperature extremes. A spring washer on the reverse side of the fin minimizes this effect by allowing the aluminum to expand against the washer compression rather than the copper.

#### 7.8.5 Clamping Pressure (Disc Type)

A self-leveling type mounting clamp is recommended to assure parallelism and even distribution of pressure on each contact area. A swivel type clamp will apply the mounting pressure in the desired manner; other configurations such as a narrow leaf spring in contact with the heat dissipator, can provide acceptable performance. Also the material thickness of the heat dissipator must be sufficient to make possible uniform pressure over the contacting surfaces.

The clamping pressure should be applied gradually, evenly and perpendicularly to the semiconductor device to ensure that there is no deformation of either the device or the heat dissipator mounting surfaces during installation. The spring used should provide a mounting pressure within the range recommended by the semiconductor device manufacturer.

#### 7.8.5 (continued)

When installing an assembly of a disc type semiconductor device mounted between two heat dissipators, it should be done in a manner to permit one heat dissipator to move with respect to the other. This will avoid stresses being built up, due to thermal expansion, which could damage the semiconductor junction. However, the clamping structure must be such that proper pressure is maintained throughout the operating temperature range of the system.

Similarly, when two or more disc type devices are to be operated electrically in parallel, one of the heat dissipators used may be common to all the devices, but it is preferred practice to provide individual heat dissipators against the other mounting surfaces of the semiconductor devices so that the mounting force applied in each case is independent of the force(s) applied to the other(s).